Ultrathin Thermoelectric Devices for On-Chip Peltier Cooling

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***Abstract*— The efficient usage of thermoelectric (TE) devices for microelectronics cooling application requires investigation and remedy of various obstacles such as integration of these devices with electronic package, parasitic contact resistances, and utilization of appropriate current pulses. We develop a computational model to investigate the effect of steady state and transient mode of operation of ultrathin thermoelectric cooler (TEC) devices on hot-spot cooling considering the effect of crucial thermal and electrical contact resistances. Our analysis shows that the transient pulses can be very effective in reducing the hot-spot temperature by 6–7 °C in addition to the cooling achieved by the steady state current through the TEC device. We correlate the important characteristics of the transient temperature behavior of hot-spot under the TEC operation such as the maximum temperature drop (ΔT_{max}), time taken to achieve ΔT_{max} and temperature overshoot after turning off pulse current with the electrical and thermal contact resistances and Seebeck coefficient of the TE material. It has been observed that thermal and electrical contact resistances play a very crucial role in the performance of TEC devices as high values of these resistances can significantly diminish the effect of Peltier cooling during steady state operation. The effect of these parasitic resistances is even higher for the transient cooling of hot-spots by the pulsed current through the TEC device. High Seebeck coefficient of TE materials is desirable as it increases the figure of merit of TE devices. However, cooling capabilities of heat sink may become bottleneck to realize the benefits of very high Seebeck coefficient as the back heat flow from the hot side to cold side of TEC device diminishes the degree of cooling achieved by these ultrathin TECs.**

***Index Terms*— Contact resistance, hot-spot, Peltier, thermoelectric, transient.**

I. Introduction

THERMOELECTRIC (TE) devices have potential to make important contributions in various applications such as solid-state cooling, waste heat recovery, refrigeration, and heat pumps which may help to reduce green house emissions and provide cleaner forms of the energy generation [1]–[3]. These devices have great appeal for site-specific and on-demand cooling in microelectronic and optoelectronic devices [1], [4]. The power distribution on a microelectronic chip could be highly non-uniform both on temporal and local scales, which could lead to hot-spots. The peak temperature on the chip drives the system level cooling solution. The conventional cooling solutions for the electronics devices are bulky and inefficient to handle localized high heat fluxes and hot-spots [1]. Thermoelectric coolers (TECs) could be employed for these applications for an efficient removal of localized heat, which may boost the performance of semiconductor devices and increase the operating life of electronic circuits [5]–[7].

Despite high appeal in terms of operational simplicity, usage of TE devices for various commercial applications is limited due to the low efficiency and high cost compared with the conventional technologies. A figure of merit $ZT = \sigma S^2 T/k$ expresses the efficiency of TE materials where σ is the electrical conductivity, S is the Seebeck coefficient, k is the thermal conductivity, and T is the operating temperature [8]. A wide range of alloys and superlattices of different materials such as SiGe, Bi_2Te_3, Sb_2Te_3, and skutterudites have been rigorously investigated to improve the figure of merit, ZT [7], [9]–[11]. The additional challenges for TEC usage in electronic cooling applications are low heat-flux pumping capacity and non-disruptive integration with the electronic devices. High electrical and thermal contact resistances further degrade the performance of these devices [1].

Significant efforts have been made in recent years to explore TECs for cooling hot-spots in microprocessors. In a related study, Litivinovitch *et al.* have analyzed steady state cooling of hot-spot using both Si and SiGe superlattice TECs [12]. They observed a maximum cooling of 4.5 °C at the hot-spot location using TECs. Additional cooling over steady state values can be achieved for a short period of time at hot-spot using transient current pulses. Pulse cooling effect in TECs has been known for few decades and has been studied extensively for free standing TECs. This effect is attributed to the interplay between Peltier cooling (surface effect) and Joule heating (volume or bulk effect) as the former effect is realized quicker at the cold junction compared to the later. Diffusion time constant for Joule heating in TEC devices can be order of magnitude higher than that of Peltier cooling (~10–20 μs). The difference in these two time scales can be utilized for the transient cooling on the chip as a lower than steady state temperature can be achieved momentarily at the colder surface [8].

Transient cooling performance of TECs depends on several parameters such as the TE material, TEC geometry, pulse

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current characteristics (shape, duration and amplitude) etc. Experimental and numerical investigation of the transient pulse mode cooling by TEC devices has been studied by Snyder *et al*. [8]. They explored various parameters such as current pulse amplitude, thermal diffusivity, supercooled temperature, and time to reach the minimum temperature. A 3-D theoretical model was proposed by Cheng *et al*. [13] to simulate transient thermal behavior of TECs. They found that the coefficient of performance (COP) (which is defined as the ratio of heat removal from cold junction to energy consumed by TEC) of TEC increases with increase in the cooling load for a given current. Yang *et al*. [14] have performed a numerical analysis of transient response of TECs with and without a cooling load attached to the TEC. They suggested that the pulse duration should be chosen based on the characteristic time constants for efficient pulsed cooling. Thonhauser *et al*. [15] studied the influence of pulse shape during transient mode operation and found that a quadratic pulse form is the most efficient as it consumes less energy and prevents extensive heating. An electrical analogue of the 1-D transient model of TEC was proposed by Mitrani *et al*. [16] to study the pulse cooling using SPICE. They investigated the effect of pulse shape and magnitude on cooling and analyzed the associated characteristic time constants. Harvey *et al*. [17] studied the effect of managing individual thermocouples inside TEC on the efficiency of TECs while cooling a chip. They suggested that significant gains in performances in terms of the energy efficiency can be realized using distributed control of TEC.

Most of the studies based on the transient mode of operation have been performed for free standing thick TECs where contact resistances are not crucial. Recently, TEC modules made of ultrathin ($\sim$100 μm) Bi_2Te_3 based superlattices have been successfully integrated to the heat spreader of an electronic package for site-specific localized cooling [1]. The cooling capacity of TECs can be significantly improved by employing these ultrathin TEC modules as it improves the heat pumping capacity and has the potential to be integrated on the active side of the chip. Wang *et al*. [18] conducted numerical and experimental study for on-chip hot-spot cooling using mini-contact TECs and observed that high thermal contact resistance can have detrimental effect to the extent that it can completely nullify the cooling effect. Ju [19] performed numerical investigation of pulse cooling in 1-D TEC geometry to study the effect of contact electrical resistance on its performance. They observed that the intense localized heating at the interface due to the electrical contact resistances strongly affects the minimum achievable temperature at the cold junction. The author further suggested that the impact of electrical contact resistance can be more pronounced for the TECs of length of the order of 100 μm or smaller.

The past studies on pulsed cooling are mostly based on the 1-D geometries isolated from the realistic electronic package. A detailed study of the pulsed cooling in the context of use of ultrathin TEC modules on the active side of the electronic package considering the details of 3-D package and TEC device has not been performed. Transient cooling by TEC devices involves two competitive effects, Joule heating and Peltier cooling. Peltier cooling is a surface effect, which helps in reducing hot-spot temperature by removing heat from the cold junction. Whereas, Joule heating is a volumetric effect and it increases temperature not only within TEC but also at the hot-spot. The spatial difference between the origins of these two effects allows Peltier cooling effect to be realized at the hot-spot location earlier than the joule heating effect. Short current pulses through TECs can help to extract the advantage of this phenomenon. However, the effect of parasitic contact resistances at the interface of TE material and metallic layers inside an ultrathin TEC module and at the interface of TEC module and package can significantly affect the TEC performance in a transient operation. A detailed investigation is required to quantify how these parasitic resistances degrade the TEC performance. The degree of Peltier cooling is directly proportional to the Seebeck coefficient of TE material. However, high temperature gradient across TE material can lead to back flow of heat and the range of desired Seebeck coefficient need to be investigated. Finally, the high energy consumption and low efficiency is one of the major obstacles for the TEC employment in the electronic cooling applications. It is crucial to explore whether ultrathin TECs provide any significant advantage in reducing the power consumption. The goal of this paper is to address all important issues related with the ultrathin TEC operation in the electronic package environment discussed above.

In this paper, we develop a detailed 3-D thermal model of the electronic package and attached TEC devices to investigate the effect of both steady state and transient mode of operation of TECs on hot-spot temperature. Our numerical model solves for the temperature distribution in the electronic package and TEC modules including the effect of thermal and electrical contact resistances, which are very significant for the ultrathin TEC modules. We incorporated the effect of Peltier cooling and Joule heating inside the TEC module to analyze the temperature reduction at hot spot on the chip for current pulses of different magnitudes. Important contributions of this paper are listed as follows.

1) The effect of parasitic contact resistances for ultrathin TEC devices integrated with a 3-D electronic package is investigated for the steady-state and transient operation of TECs, which provides insights for the range of acceptable or desired contact resistances in order to efficiently use these devices.
2) The important characteristics of the transient temperature behavior of hot spot under the TEC operation such as the maximum temperature drop ($\Delta T_{\max}$), time taken to achieve $\Delta T_{\max}$ and the temperature overshoot after turning off a pulse current have been investigated and empirical correlations have been derived, which correlate these characteristics with the vital parameters such as the amplitude of pulsed current, electrical and thermal contact resistances, etc. These correlations will provide the guidelines for the design of current pulses and control algorithms in order to facilitate smooth operation of TECs.
3) The effect of Seebeck coefficient on pulse cooling has been discussed, which describes the limits of high values of Seebeck coefficient to avoid excessive back heat

flow. The energy analysis of TEC operation has been presented to explore the energy consumed for a specified heat removal by these ultrathin TEC devices and hence reveal the COP of these devices.

The rest of this paper is organized as follows. Section II explains the governing equations for the TEC operation, computational model, and the validation of the model against published experimental measurements. In Section III, the key parameters, their importance and their range of study is described, which is followed by the results and analysis. Finally, Section IV concludes this paper.

II. Computational Methodology and Validation

We develop a computational model which solves Fourier's conduction equation in the electronic package and TEC module to analyze the effect of TEC device on temperature reduction at hot-spot location on a chip. A schematic of the electronic package, TEC module, and heat sink is shown in Fig. 1. A 100 μm thick TEC module comprised of 7 $\times$ 7 p-n couples is attached at the back side of the heat spreader. The area of the TEC device is 3.5 mm $\times$ 3.5 mm. The thickness of the TE layer of the TEC device is 8 μm; two metallic layers are attached on the both sides of this thin layer. We have selected this geometry to compare and validate our modeling results against the steady state experimental and computational results in [1]. The reference values of electrical/thermal contact resistances at the interface of superlattice–metal layer (10^{-11} Ωm^2; 1×10^{-6} m^{2}K/W) and at the interface of TEC module-heat spreader layer (10^{-10} Ωm^2; 8×10^{-6} m^{2}K/W) are also obtained from [1]. These values of contact resistances are considered in all simulations unless stated differently. The dimensions and thermal conductivity of different components of the electronic package and TEC module are listed in Table I. Our computational domain includes heat spreader, thermal interface material (TIM), chip, and TEC. In order to reduce the computational time of the simulation, the heat sink is represented by a convective heat transfer boundary condition at the top of the spreader surface. A high heat flux (1250 W/cm^2) source is located at the center of the bottom surface of chip (area 400 $\times$ 400 μm^2), which generates a hot spot at the center. The rest of the bottom surface is considered as heat source of uniform heat flux of 43 W/cm^2. These values of heat fluxes at the bottom of the chip are chosen in order to compare our numerical results against the experimental observations in [1].

The operation of TECs is based on the interplay of Peltier cooling and Joule heating. Note the Peltier cooling is a surface effect while the Joule heating is a volume effect. Heat is absorbed at one side of the TEC module (cold-junction) when a TEC module is turned on and rejected at the other side of the module (hotter junction). We incorporate the Peltier cooling effect by adding heat ($\sim$S$\cdot$I$\cdot$T$_h$) at the hotter side and subtracting heat ($\sim$S$\cdot$I$\cdot$T$_c$) from the colder side of the superlattice structures. Here, T$_h$ and T$_c$ are the temperatures of the hotter and colder junctions. The value of S is taken as 300 μV/K based on the experimental measurement in [1]. The volumetric heat generation inside the TEC layer, at the interface of the superlattice and metal layer and at the interface

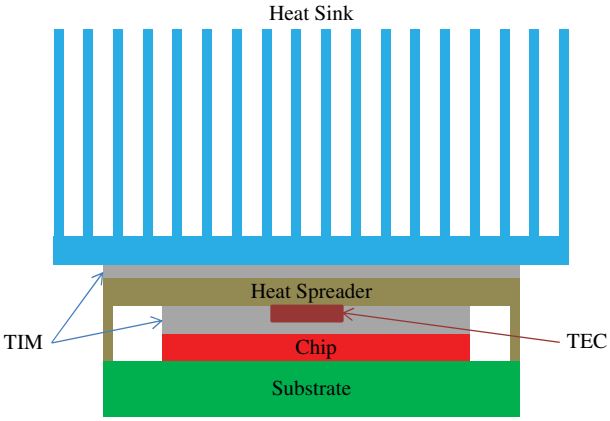


Fig. 1. Schematic of an electronic package. Heat spreader, chip, TIM, chip, substrate, and TEC are shown.

TABLE I
Dimensions and Thermal Conductivity of Different Components of the Electronic Package

Component	Thermal Conductivity (W/m-K)	Dimensions
Spreader	400	30 mm $\times$ 1 mm $\times$ 30 mm
TIM	1.75	11 mm $\times$ 0.125 mm $\times$ 13 mm
TEC-superlattice	1.2	3.5 mm $\times$ 0.008 mm $\times$ 3.5 mm
Chip	140	11 mm $\times$ 0.5 mm $\times$ 13 mm

of TEC module and heat spreader layer is considered by adding Joule heating terms (I^2R) terms at the corresponding volumes and layers. The thermal contact resistances at these interfaces are incorporated by adding an appropriate thermal resistor at the corresponding interfaces.

1) Governing Equations: The governing differential equation for temperature distribution inside the electronic package is represented as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \dot{Q} = \frac{\partial T}{\alpha \partial t} \tag{1}$$

where

$$\dot{Q} = \begin{cases} \frac{I^2}{A^2 \sigma k} & \text{inside TEC} \\ 0 & \text{elsewhere.} \end{cases} \tag{2}$$

Here, T is temperature, α is thermal diffusivity, I is current, A is area of an element, σ is electrical conductivity, and k is thermal conductivity.

2) Boundary Conditions: Heat flux boundary condition is applied at the bottom of the chip, which can be expressed as

$$-k\frac{\partial T}{\partial y} = q'' \quad \text{where} \quad q'' = \begin{cases} 1250 \frac{W}{\text{cm}^2} & \text{at the hot spot} \\ 43 \frac{W}{\text{cm}^2} & \text{elsewhere.} \end{cases} \tag{3}$$

In addition, at the cold end of TEC

$$-kA \left.\frac{\partial T}{\partial y}\right|_{y=y_c^+} = \left[-kA\frac{\partial T}{\partial y} - SIT\right]_{y=y_c^-} + I^2 R_{elec}. \tag{4}$$

Here, the y coordinate is directed from TEC to the heat spreader, and y_c^+ and y_c^- are locations just above and below the cold junction. S is Seebeck coefficient and R_{elec} is contact electrical resistance.

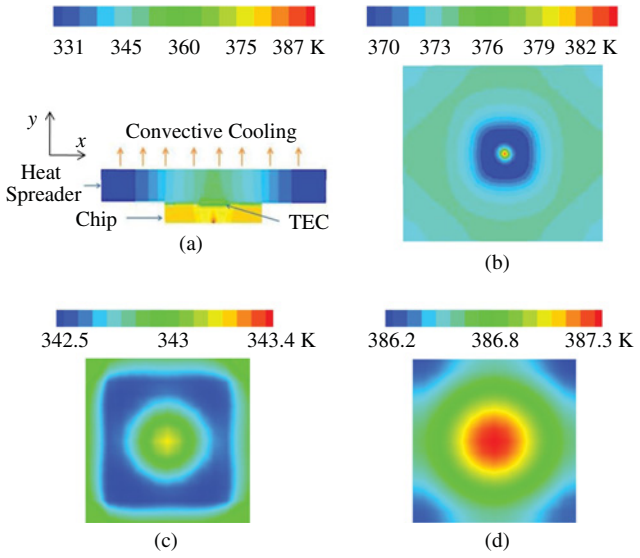


Fig. 2. (a) Temperature contours in a vertical cross-section of an electronic package are shown [only heat spreader, TIM, chip, substrate, and TEC is considered for simulations. Convective heat transfer boundary condition is applied at the top of the spreader]. (b) Temperature contours on the bottom surface of the chip. High heat flux (1250 W/cm^2) source is located at the center of this surface of area 400 × 400 μm^2 which generate a hot spot at the center. The rest of the surface has a uniform heat flux of 43 W/cm^2. (c) Temperature contour at the cold side of TEC. (d) Temperature contour at the hot side of TEC.

Also, at hot end of TEC

$$-kA\left.\frac{\partial T}{\partial y}\right|_{y=y_h^+} = \left[-kA\frac{\partial T}{\partial y} + SIT\right]_{y=y_h^-} + I^2 R_{elec} \quad (5)$$

y_h^+ and y_h^- are locations just above and below hot junction.

Finally, at the top surface of heat spreader

$$-k\frac{\partial T}{\partial y} = h(T - T_\infty). \quad (6)$$

Here, h is convective heat transfer coefficient and T_∞ is ambient air temperature, which is taken as 300 K.

The simulations are performed using the finite volume method-based commercial solver FLUENT. 200 K cells are considered for the simulations, grid independence tests verify that these cells are sufficient for the further simulations. The temperature contours in a vertical cross-section of the electronic package, on the chip bottom surface and at the cold and hot sides of TEC are shown in Fig. 2.

The computational model is validated by comparing the hot spot temperature at the bottom surface of the chip against the numerical results in [1], which was verified against the experimental observations in [1]. The comparison is done with and without considering the contact thermal and electrical resistances at the superlattice–metal interface. An excellent agreement (within 2–3 °C) with the results in [1] for different values of contact resistances validates the developed computation model (Fig. 3). The maximum cooling (5.5 °C) at steady state is achieved at the current amplitude of 3 A, which is also observed in the experimental measurements in [1].

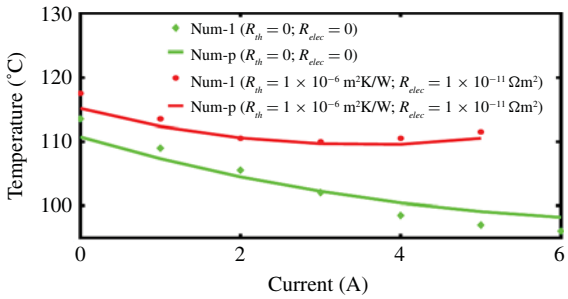


Fig. 3. Hot-spot temperature at the bottom surface of the chip is compared with the numerical results in [1], which was verified against the experimental observations in [1]. Here, 'Num-1' corresponds to the numerical results in [1] and 'Num-p' corresponds to the current simulation results.

III. Results and Discussion

A. Range of Important Parameters

The important parameters investigated in this section are thermal (R_{th}) and electrical (R_{elec}) contact resistances at the interfaces of TE material and the metallic layers inside the TEC module and the Seebeck coefficient (S) of TE material. Thermal contact resistance is a very important parameter as it can be a major contributor of TEC total thermal resistance leading to the bottleneck for effective heat removal from the hot side of the TEC module to the ambient which in turn can increase the temperature at the cold junction of TEC and at the hot spot. The range of the thermal contact resistances considered in this paper is 1 × 10^{-7}–7.5 × 10^{-6} m^{2}K/W. These resistances are dependent on the fabrication process and can vary from one manufacturing process to the other. The range of R_{th} considered here is based on the typical value of thermal contact resistances estimated in [1]. The electrical contact resistance at the TE-metal interface leads to the Joule heating which can drastically diminish the effect of the Peltier cooling. In this paper, we consider the effective TE properties of the Bie_2Te_3 based thin film TE material which makes Ohmic contact with the metallic layers inside the TECs. The typical values of R_{elec} measured in [1] using transmission line method is of the order of 10^{-11} Ωm^2. However, these values are largely dependent on the fabrication process, so we consider R_{elec} in the range of 10^{-12} Ωm^2 to 10^{-10} Ωm^2. We have derived the empirical correlations between the transient temperature characteristics at the hot spot and R_{th}/R_{elec} values to provide guidelines for the future design of TEC operation. Seebeck coefficient (S) is another important parameter investigated in this paper. High S values are desired in TE applications as the figure of merit of TE materials is proportional to the square of S. Designing materials with high S and hence high figure of merit is very active research area in the materials science. However, high Seebeck coefficient can also have an adverse effect on hot-spot cooling as back heat flow in TEC device can diminish the effect of Peltier cooling and so the investigation of effects of S on the degree of achieved cooling is important. The value of S for Bie_2Te_3 superlattice material is measured as 300 μV/K in [1]. In this paper, it has been varied between 100 μV/K to 400 μV/K to study the effect of extreme values during

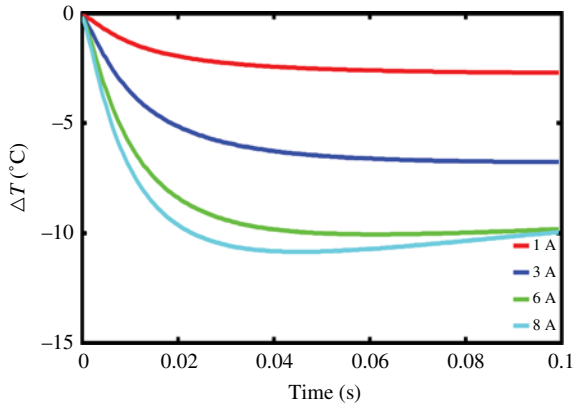


Fig. 4. Hot-spot temperature change with time after turning on TEC device at different current amplitudes.

steady-state and transient operation. For the parameters and their ranges discussed above, we analyze both steady state and transient operation of TECs and investigate the effect of amplitude of current pulses and the energy consumption in TEC devices.

B. Transient Response of Hot Spot

The lower response time for the Peltier cooling compared to the Joule heating can allow high amplitude transient current pulse through the TEC device to reduce the temperature at the hot-spot below the steady state operation of TECs. This transient mode operation of TECs may lead to very efficient on-demand cooling of hot spots in the microelectronic chips. We first investigate the change in hot-spot temperature with time after turning on the TEC device at different current amplitudes. Lower values of current amplitude demonstrate the dominance of Peltier cooling effect due to the relatively low Joule heating. For low values of current amplitudes ($\leq$3 A), the hot-spot temperature stabilizes and achieves its steady state values in less than 0.1 s. For higher amplitude currents ($\geq$6 A), Joule heating becomes significant and can counter the Peltier cooling effect. This suggests that temperature at hot spot should reduce first due to Peltier cooling, reach a minimum value and subsequently increase when Joule heating effects is realized at the surface, which is typically realized slower than the Peltier cooling. The numerical results confirm this behavior as the maximum cooling does not correspond to the steady state values but at some intermediate time (e.g. 0.03 s for $I = 8$ A), Fig. 4. It should be noted that the effect is realized at the hot spot on the chip bottom surface, which is located 0.5 mm away from the location of the colder side of TE superlattice. This clearly indicates that TEC can be utilized for the additional transient cooling at the hot spot.

We next explore the effect of transient current pulses on Peltier cooling by applying pulses of different magnitudes (I_p) on top of the constant current ($I_{\min}$) through the TEC device and investigate the characteristics of transient temperature behavior at hot spot in response to the pulsed current through the TEC. The transient current pulses of period 0.06 s are applied after the system temperature reaches to their steady state values at constant current of $I_{\min}$. Here, $I_{\min} = 3$ A

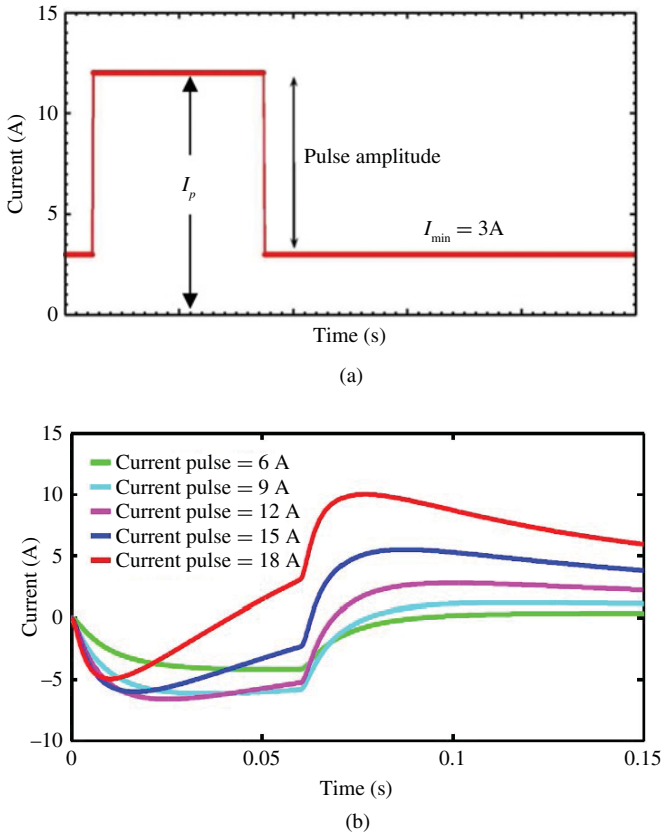


Fig. 5. (a) Shape of the current pulse for $I_p = 4 \times I_{\min} = 12$ A. (b) Temperature drop at hot spot with time subjected to a pulsed current of 0.06 s duration for different values of I_P. The current pulse is applied after the system reaches steady state at $I_{\min} = 3$ A.

is the current magnitude, which provides maximum steady state cooling (T_{ss}) (see Fig. 3). The shape of the current pulse is shown in Fig. 5(a). Fig. 5(b) shows the change in additional cooling ($\Delta T = T - T_{ss}$) achieved at hot-spot location with time for transient current pulses of different magnitudes (defined as I_p in the figure). After reaching minimum temperature at the hot spot, temperature starts rising and overshoot in temperature over the steady state values is observed even though the current pulse amplitude is changed back to $I_{\min} = 3$ A. Three important characteristics of the observed transient cooling at hot-spot location subjected to transient pulse is the maximum temperature drop ($\Delta T_{\max}$), the time taken to achieve maximum temperature drop ($t_{\min}$), and the temperature difference ($\Delta T_{\text{overshoot}}$) between peak value of the temperature attained at hot spot after the pulse current is turned off and the steady state temperature (T_{ss}). Next, we derive and analyze the empirical correlations for these temperature characteristics of transient cooling for current pulses of different amplitudes.

1) Empirical Correlations: The empirical correlations for transient temperature characteristics are important as they can provide guidelines for the design of the current pulses in order to facilitate smooth and energy efficient operation of TECs. The time ($t_{\min}$) taken to achieve maximum temperature drop at hot spot during pulse cooling decreases as the current pulse amplitude is increased which means higher I_P corresponds to faster cooling [Fig. 6(a)]. An expression for $t_{\min}$ is derived

using linear approximation of 1-D heat equation for TEC in [8], i.e., $t_{\min} \sim [I_P/I_{\min} + 1]^{-2}$. Our numerical data are proportional to a slightly changed expression $[I_P/I_{\min} + 2]^{-2}$. This difference can be attributed to the fact that $t_{\min}$ in our analysis corresponds to the location of hot spot, which is away from TEC cold junction and our analysis corresponds to a 3-D system while expression for $t_{\min}$ in [8] corresponds to the temperature at cold junction of an isolated TEC. $\Delta T_{\max}$ increases with increasing I_P due to the augmented Peltier cooling but soon attains a peak value of 6 °C corresponding to $I_p = 12$ A and subsequently $\Delta T_{\max}$ starts decreasing as the increasing Joule heating effect with increasing current diminishes Peltier cooling effect at hot spot, Fig. 6(b). These results suggest that higher values of I_P (>12 A) are not favorable as they bring down $\Delta T_{\max}$ and reduce the cooling duration as well.

Empirical formulae for $t_{\min}$ and $\Delta T_{\max}$ are expressed by (7) and (8), these correlations give a close fit to the numerical data, which relate $t_{\min}$ and $\Delta T_{\max}$ to current pulse ratio $(I_P/I_{\min})$ when other parameters are kept constant

$$t_{\min} = 0.8\left(\frac{I_p}{I_{\min}} + 2\right)^{-2} \tag{7}$$

$$\Delta T_{\max} = 7\left[1 - \exp\left(1 - \frac{I_p}{I_{\min}}\right)\right]. \tag{8}$$

It is interesting to note that this paper is focused on the cooling of hot spot located below the cold end of TEC at some distance inside 3-D electronic package and yet the empirical expression for $\Delta T_{\max}$ and $t_{\min}$ are similar to that obtained by Snyder *et al*. [8] who performed the study for free standing 1-D TEC. Temperature overshoot ($\Delta T_{\text{overshoot}}$) is the temperature difference between peak value of the temperature at hot spot after the pulse current is turned off and T_{ss}; it increases as the current pulse magnitude is increased [Fig. 6(c)]. Pulsed current duration also affects $\Delta T_{\text{overshoot}}$ significantly. Results suggest that current pulse should be turned off just after achieving $\Delta T_{\max}$ in order to minimize $\Delta T_{\text{overshoot}}$.

C. Thermal Contact Resistance Effect

In this section, we analyze the effect of thermal contact resistance at the interface of TE material and metallic layers in a TEC device for both steady and transient operation of TEC. The analysis also provides insights for the range of acceptable or desired contact resistances for the efficient usage of TEC devices. Since, the Peltier effect originates at the surface, the role of contact thermal resistances during TEC operation becomes very important as these contact resistances in ultrathin TEC device can significantly degrade the performance. A significant variation in these resistances is possible depending on the fabrication process and attachment method of TEC devices with the electronic package. We analyzed the effect of these resistances by changing the thermal contact resistance (R_{th}) in the range of 1×10^{-7}–7.5×10^{-6} m^{2}K/W; the typical value of contact resistance estimated in [1] is 1×10^{-6} m^{2}K/W. The degree of cooling achieved by applying steady state current through the TEC is shown in Fig. 7(a). The maximum achievable cooling at hot spot decreases from

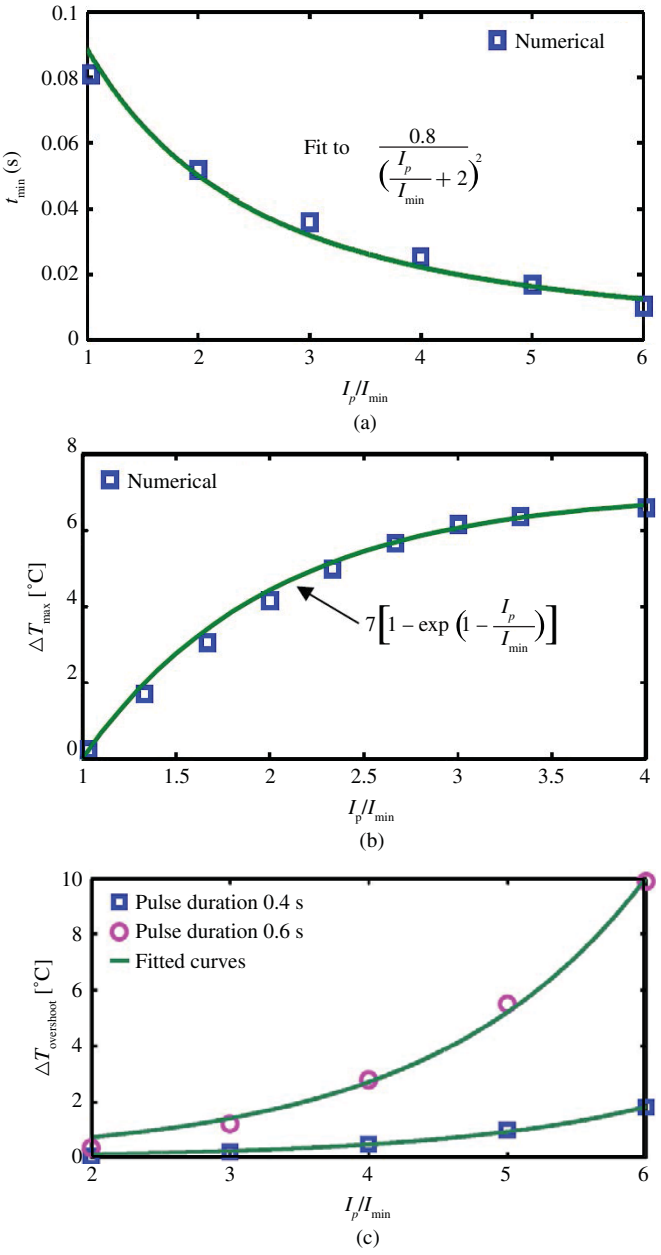
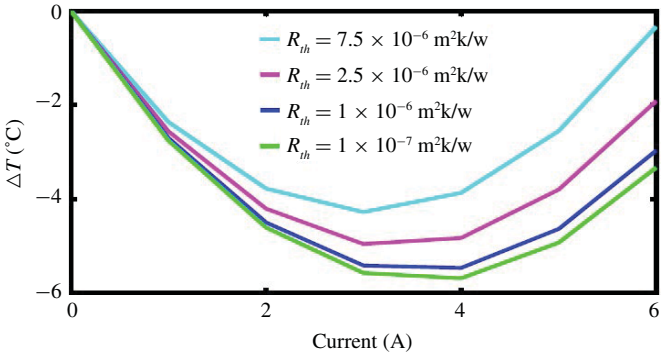


Fig. 6. (a) Time to reach minimum temperature ($t_{\min}$) at hot-spot location for current pulses of different magnitudes and duration 0.04 s. (b) Variation of maximum temperature drop ($\Delta T_{\max}$) at hot spot subjected to current pulses of 0.04 s duration. (c) Temperature overshoot at hot spot subjected to pulsed current of two different durations (0.4 s and 0.6 s). $I_{\min} = 3$ A.

5.5 °C to 4 °C when R_{th} is increased from 1×10^{-7} m^{2}K/W to 7.5×10^{-6} m^{2}K/W. The maximum cooling corresponds to the different current amplitudes for different R_{th}. Decreasing R_{th} allows applying high amplitude currents in order to achieve best cooling at the hot spot, Fig. 7(a).

1) Transient Cooling and Empirical Correlations: The effect of R_{th} on the additional cooling achieved by the application of transient pulses is even worse. The additional cooling (ΔT) achieved by applying a pulsed current of $I_p = 12$ A and 0.04 s duration is shown in Fig. 7(b). We analyze the transient thermal characteristics of this additional cooling, $t_{\min}$, $\Delta T_{\max}$, and $\Delta T_{\text{overshoot}}$ as function of R_{th}. The time to reach



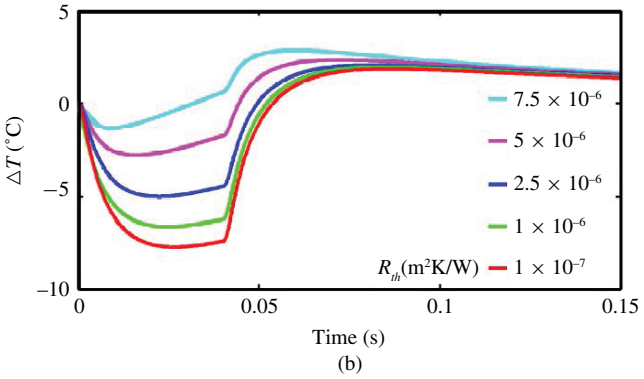


Fig. 7. (a) Steady-state (I = 3 A) temperature drop at hot spot for different thermal resistances at superlattice–metal interface. (b) Temperature drop at hot spot with time subjected to a pulsed current of 0.04s duration. The thermal resistances at superlattice–metal interface corresponding to different curves are shown in the figure. The current pulse is applied after the package reaches steady state at $I_{\min} = 3$ A. $I_p = 12$ A.

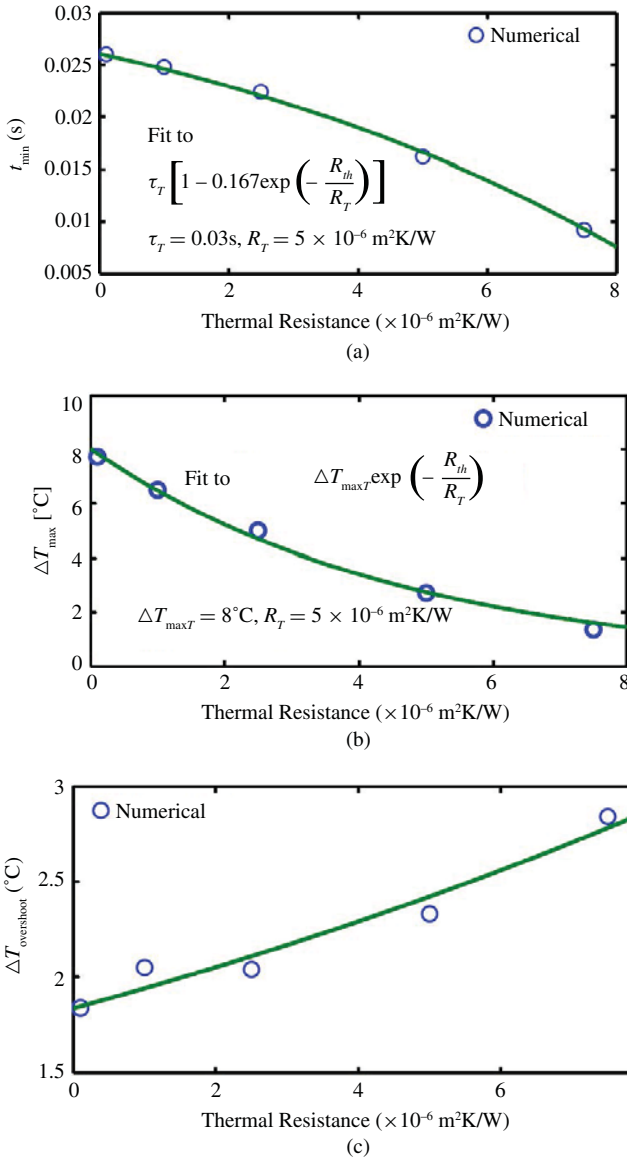


Fig. 8. (a) Variation of $t_{\min}$ for different thermal contact resistances. (b) Maximum temperature drop at hot spot for different thermal contact resistances. (c) Temperature overshoot at hot spot. Pulsed current of 12 A is used for 0.04 s duration. $I_{\min} = 3$ A.

maximum cooling ($t_{\min}$) decreases with increasing contact thermal resistances [Fig. 8(a)]. An empirically determined correlation given by (9) shows an exponential relationship between $t_{\min}$ and R_{th} when all other parameters are kept fixed. The increase in R_{th} accompanies with decrease in maximum temperature drop ($\Delta T_{\max}$). $\Delta T_{\max}$ decreases from 6.5 °C to 1 °C when R_{th} is increased from typical value of 1×10^{-6}m²K/W to 7.5×10^{-6} m²K/W, but increases by 3 °C when R_{th} is decreased from 1×10^{-6}m²K/W to 1×10^{-7} m²K/W, [Fig. 8(b)]. Clearly, an order of magnitude increase in R_{th} (from 10^{-6}m²K/W to 10^{-5} m²K/W) almost nullifies the Peltier cooling. This underlines the requirement of low parasitic resistances for the efficient utilization of TEC during transient pulsed cooling. However, decreasing R_{th} values lower than 1×10^{-7} m²K/W does not provide any further significant increase in $\Delta T_{\max}$ indicating the maximum desired value of R_{th}. The empirical correlation between $\Delta T_{\max}$ and R_{th} given by (10) also shows an exponential relationship, which can be used to estimate the effect of the parasitic resistances on the degree of cooling. The R_T in (9) and (10) can be considered as characteristic parasitic thermal resistance constant of the interface. Higher values of contact thermal resistance also augment $\Delta T_{\text{overshoot}}$. For pulse current magnitude (12 A) and duration (0.4 s), $\Delta T_{\text{overshoot}}$ increases by 0.8 °C when R_{th} is increased from 1×10^{-6} m²K/W to 7.5×10^{-6} m²K/W [Fig. 8(c)]. R_{th} has significant impact on all transient temperature characteristics and so requires a significant attention in order to keep its value as low as possible

$$t_{\min} = \tau_T\left[1 - 0.167\exp\left(\frac{R_{th}}{R_T}\right)\right], \quad \tau_T = 0.03s, \quad R_T = 5 \times 10^{-6}\text{m}^2\text{K/W} \tag{9}$$

$$\Delta T_{\max} = \Delta T_{\max T}\exp\left(-\frac{R_{th}}{R_T}\right), \quad \Delta T_{\max T} = 8\ ^\circ C, \quad R_T = 5 \times 10^{-6}\text{m}^2\text{K/W}. \tag{10}$$

D. Electrical Contact Resistance Effect

The electrical contact resistances at the superlattice–metal interface can drastically reduce the achieved cooling at the

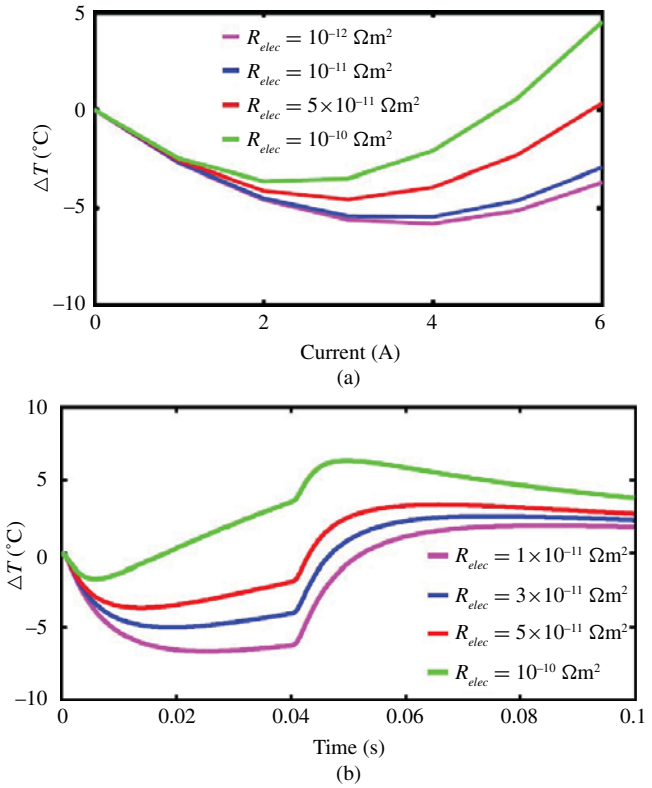


Fig. 9. (a) Steady-state (I = 3 A) temperature drop at hot spot for difference electrical resistances at superlattice–metal interface. (b) Temperature drop at hot spot with time subjected to a pulsed current of 0.04 s duration. The electrical resistances at superlattice–metal interface corresponding to different curves are shown in the figure. The current pulse is applied after the package reaches steady state at $I_{\min} = 3$ A. $I_p = 12$ A.

hot-spot location. The effect of these resistances for pulsed cooling can be more pronounced as these resistances lead to the Joule heating at the interface of superlattice–metal where Peltier cooling is the most effective. The effect of electrical contact resistances is analyzed by changing their values (R_{elec}) in the range of 10^{-11}–10^{-10} Ω-m^2 which are chosen based on the experimental measurements in [1]. The degree of cooling achieved by applying steady-state current for these different values of R_{elec} is shown in Fig. 9(a). When R_{elec} is increased from 10^{-11} Ωm^2 to 10^{-10} Ωm^2, the maximum achievable cooling at hot spot is reduced from 5.5 °C to 3.5 °C. Variation of R_{elec} from 10^{-12} Ωm^2 to 10^{-11} Ωm^2 results in very little improvement in cooling showing that an attempt to decrease electrical resistances lower than 10^{-11} Ωm^2 will not be much beneficial [see Fig. 9(b)].

1) Transient Cooling and Empirical Correlations: The effect of increasing R_{elec} on additional cooling (ΔT) achieved under the application of pulsed current is shown in Fig. 9(b). A 0.04 s long pulse with $I_p = 12$ A and steady-state current of $I_{\min} = 3$ A is applied for different values of R_{elec} at the interface. As observed for the case of thermal contact resistances, $t_{\min}$ decreases with increasing R_{elec} [Fig. 10(a)]. The numerical data for $t_{\min}$ fit well to the empirically determined exponential correlation [see (11)], which relates $t_{\min}$ to R_{elec} when other parameters are kept fixed. The maximum temperature drop $\Delta T_{\max}$ decreases from 6.5 °C to 1.5 °C when R_{elec} is increased from 10^{-11} Ωm^2 to 10^{-10} Ωm^2 [Fig. 10(b)]. The numerical data for $\Delta T_{\max}$ follow the empirical correlation given by (12) where $\Delta T_{\max E}$ is the maximum temperature drop when there is no electrical contact resistance at the interface and R_E is the characteristic contact electrical resistance of the interface, which can serve as a useful indicator for the tolerable limits of R_{elec}. It can be inferred from the results that increasing contact electrical resistance significantly degrades Peltier cooling resulting in lower values of both $t_{\min}$ and $\Delta T_{\max}$

$$t_{\min} = \tau_E \exp\left(-\frac{R_{elec}}{R_E}\right), \quad \tau_E = 0.029s, \quad R_E = 7 \times 10^{-11}\ \Omega\text{m}^2 \tag{11}$$

$$\Delta T_{\max} = \Delta T_{\max E} \exp\left(-\frac{R_{elec}}{R_E}\right), \quad \Delta T_{\max E} = 7.5\ ^\circ\text{C}, \quad R_E = 7 \times 10^{-11}\ \Omega\text{m}^2. \tag{12}$$

The higher values of contact electrical resistance also augment $\Delta T_{\text{overshoot}}$. For pulse current magnitude (12 A) and duration (0.4 s), $\Delta T_{\text{overshoot}}$ increases by 4 °C when R_{elec} is increased from 10^{-11} Ωm^2 to 10^{-10} Ωm^2 [Fig. 10(c)]. The effect of electrical contact resistances on temperature overshoot is much higher than the effect of thermal contact resistances [see Figs. 8(c) and 10(c)] indicating that a significant discretion is required to select the current pulses considering the effect of crucial electrical contact resistances in order to minimize the temperature overshoot.

E. Seebeck Coefficient Effect

We next analyze the effect of Seebeck coefficient (S) on steady state and transient operation of TEC while keeping the cooling capability of heat sink unchanged [∼constant h in (6)]. Seebeck coefficient (S) of TEC devices has significant impact on the Peltier cooling at the hot-spot location as amount of heat removed from the colder side of the superlattice structures is proportional to the value of Seebeck coefficient. High S values are desired in all TE applications. However, high Seebeck coefficient can have an adverse effect on hot-spot cooling as back heat flow in TEC device can diminish Peltier cooling effect. To quantify the effect, we first investigate the degree of cooling achieved at hot-spot for different steady-state currents and for different values of Seebeck coefficient in the range of 100–400 μV/K [see Fig. 11(a)]. We observe 2–8 °C cooling at hot-spot location as we change Seebeck coefficient from 100 μV/K to 400 μV/K. It can be noticed that the effect of increasing Seebeck coefficient is countered by back heat flow, which can be more pronounced for higher amplitude current (I >4) due to larger temperature difference between cold and hot ends of TEC [Fig. 11(a)]. It has been observed that for current amplitudes greater than 6A, the increased values of S can instead degrade Peltier cooling if cooling capability of heat sink remains same (∼ constant h). The effect of increasing Seebeck coefficient on additional cooling (ΔT) achieved under the application of a pulsed current is shown in Fig. 11(b). A 0.04 s long pulse with $I_p = 12$ A and steady-state current of $I_{\min} = 3$ A is applied for different values of Seebeck coefficient. We observe additional cooling (ΔT_{max}) of 1 °C

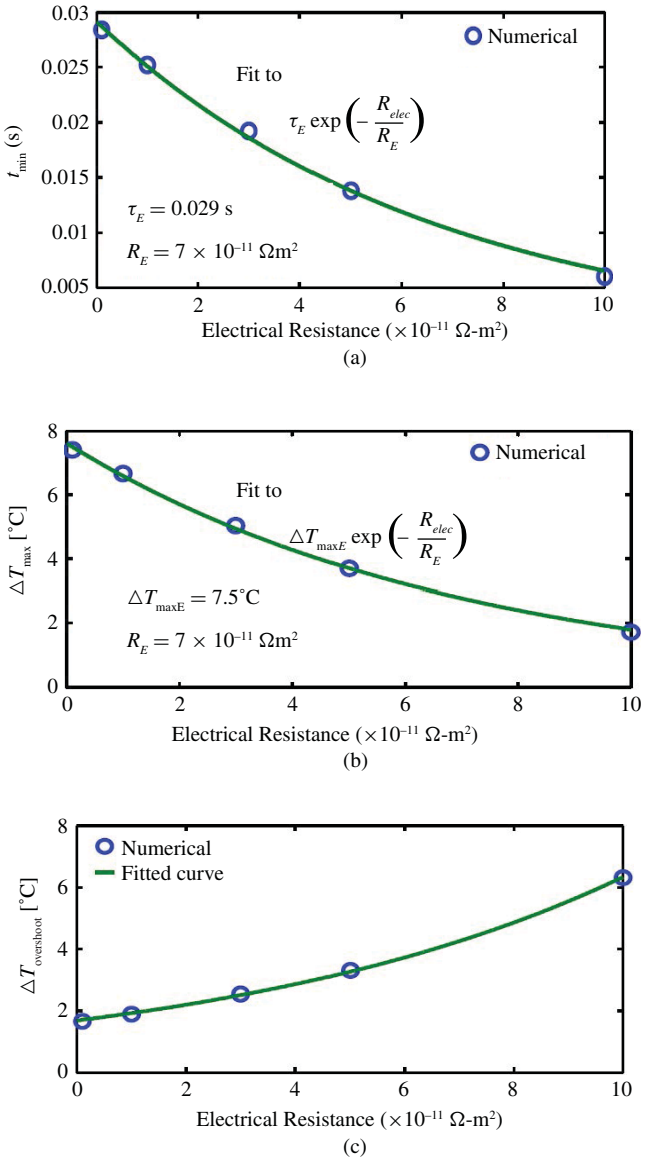


Fig. 10. (a) Variation of $t_{\min}$ for different electrical contact resistances. (b) Maximum temperature drop at hot spot for different electrical contact resistances. (c) Temperature overshoot at hot spot. Pulsed current of 12 A is used for 0.04 s duration. $I_{\min} = 3$ A.

to 7 °C when S is increased from 100 μV/K to 400 μV/K but $t_{\min}$ and $\Delta T_{\text{overshoot}}$ also increases with increasing S [see Fig. 11(b)].

Similar to the steady-state operation, values of Seebeck coefficient higher than 400 μV/K is not favorable for Peltier cooling using transient current pulses. We notice that the values of Seebeck coefficients, after which further increase in their values lead to decrease in Peltier cooling, are higher for high convective heat transfer coefficients (better cooling by heat sink). Therefore, in order to crop the benefits of high Seebeck coefficients, high cooling capability is required. Bi_2Te_3 based superlattices used in [1] for TE materials have S values of the order of 300 μV/K. The conventional air cooling solutions for electronic packages are reaching their limits and it may become bottleneck to realize the benefits of further improvement in S values of the TE materials.

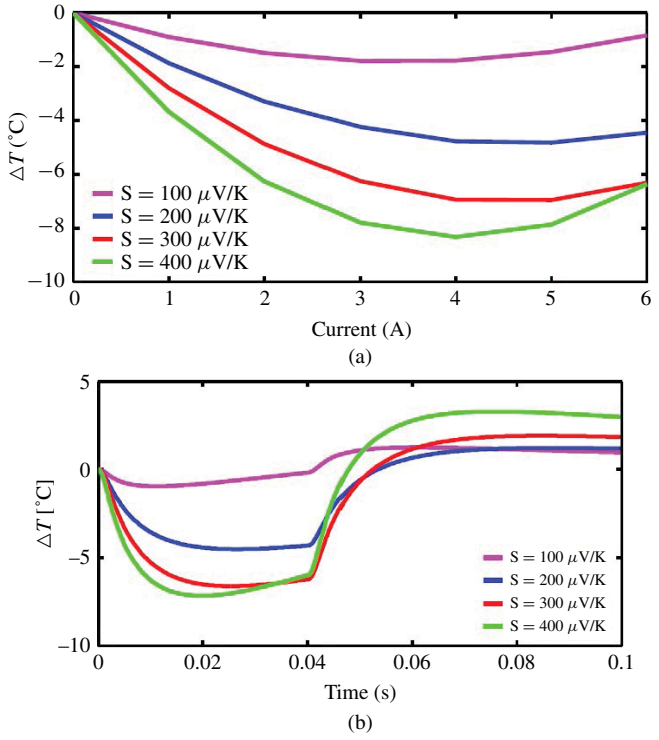


Fig. 11. (a) Steady-state temperature drop at hot spot for different values of Seebeck coefficient of TEC. (b) Temperature drop at hot spot with time subjected to a pulsed current of 0.04 s duration. Different curves correspond to different values of Seebeck coefficient as shown in the figure. The current pulse is applied after the package reaches steady state at $I_{\min} = 3$ A. $I_p = 12$ A.

F. Energy Analysis for TEC Operation

This section explores the amount of heat removed from the hot-spot as well as total heat through the cold side of TEC and the energy consumed in TEC device operation for different current amplitudes; this analysis can be further used to estimate the COP of Peltier cooling using these ultrathin TEC devices. The COP of TECs is defined as the ratio of the amount of heat removed from the hot spot to the amount of energy supplied to TEC. The amount of heat removed from the hot spot is defined as the difference of total heat from the bottom of TEC module with hot-spot on the chip and without hot spot on the chip. This is different from the total heat (Q_{in}) passing through the cold side of TEC module. The decreasing trend of COP with increasing current is shown in Fig. 12(a).

The energy supplied to TEC (ΔQ) increases parabolically with increasing current [Fig. 12(b)]. However, the heat passing through the colder side of TEC (Q_{in}) does not increase monotonically with current. It achieves a maximum value corresponding to 12 A current and then decreases because of the back heat flow as a consequence of the larger temperature difference between the hot and cold sides of TEC. The value of Q_{in}, ΔQ, and COP corresponding to the point of maximum steady-state cooling (~3 A current) are 11.8 W, 0.6 W, and 1.7, respectively. A high value of COP is noted here compared to the typical experimental values because ΔQ accounts only for the TEC power consumption, however, there might be some losses in the peripheral circuit elements which would lower the COP. Results suggest that the rate of energy taken out by TEC

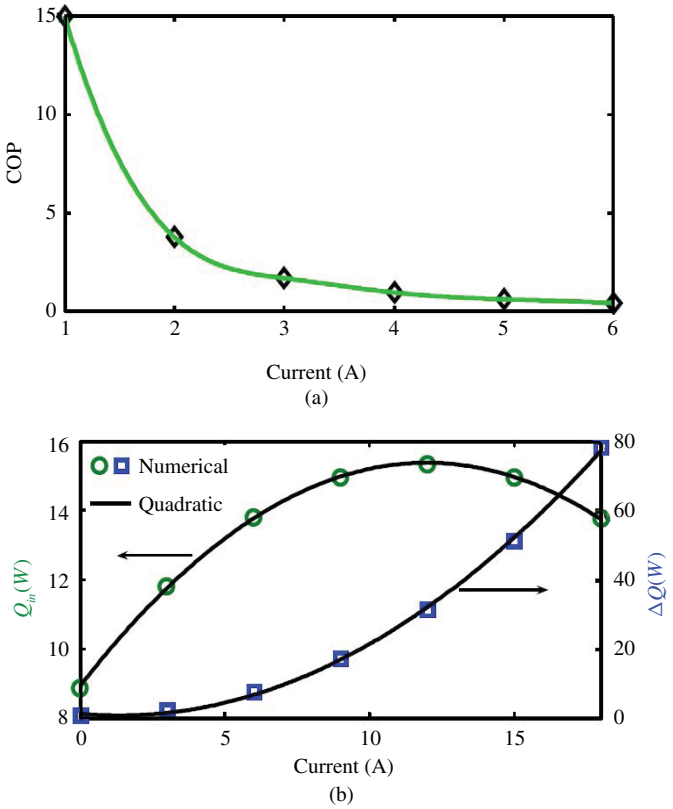


Fig. 12. (a) COP variation with current. (b) Variation of energy removed (Q_{in}) from the colder side (left axis) and energy consumed (ΔQ) by TEC (right axis) against current.

from the hot-spot is nearly 1 W and it increases slightly with increase in current. Since the power dissipated at the hot spot is 2 W, it suggests that only half of it is taken out by TEC. During pulsed cooling, the maximum temperature drop is observed for 12 A current. This current amplitude also corresponds to the maximum heat removal from the cold side as further increasing current lead to decreased Q_{in} [Fig. 12(b)]. The present energy analysis shows that the TEC-based cooling is energy efficient only for low values of the current amplitudes.

IV. Conclusion

In summary, we developed a computation model to analyze the cooling of hot spots on-chip using an ultrathin Peltier cooler, which is attached at the bottom side of the heat spreader. We investigated the effect of both steady state and transient mode of operation of TEC for hot-spot temperature reduction. The analysis shows that transient pulses can be very effective to reduce the hot-spot temperature by 6–7 °C in addition to the cooling achieved by the steady-state current pulse through the device. The efficient utilization of these pulses for transient cooling operation requires a careful optimization of shape and duration of the pulse. We observe that the effect of additional transient cooling can be diminished to 1 °C if the thermal or electrical contact resistance is an order of magnitude higher than the currently estimated values from recent experimental measurements. It was noticed that the Peltier cooling is enhanced by the increased values of Seebeck coefficient both for the steady state and pulsed cooling. However, the cooling effect of increasing Seebeck coefficient is countered by the back heat flow, which can be more pronounced for the higher values of current ($I > 4$A) due to the larger temperature difference between the cold and hot ends of TEC. In order to further enhance the energy efficiency of the Peltier cooling on a chip, a dynamic control mechanism is required which is under investigation.

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