Self-consistent electrothermal analysis of nanotube network transistors

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We develop an electrothermal transport model for nanocomposite thin films based on self-consistent solution of drift-diffusion and Poisson equations for electrons coupled with diffusive transport of heat. This model is used to analyze the performance of an electronic display the pixels of which are controlled by carbon nanotube (CNT) network thin-film transistors (TFTs). The effect of electrothermal coupling on device performance and steady state temperature rise is analyzed as a function of key device parameters such as channel length, network density, tube-to-substrate thermal conductance, and tube-to-substrate thermal conductivity ratio. Our analysis suggests that device on-current I_{on} may reduce by 30% for a 1 μm channel length devices due to self-heating. The temperature rise in such devices can be as high as 500 K in extreme cases due to the thermally insulating substrate and the low tube-to-substrate thermal conductance. These results suggest that an appropriate combination of network density, channel length and width should be selected for CNT-TFTs to avoid device temperature rise above acceptable limits. We analyze the effectiveness of active cooling in reducing the temperature and enhancing the performance of the device. We find that the high thermal spreading resistance between the CNT device and the electronic display reduces the effectiveness of forced convective cooling, necessitating the exploration of alternative designs for viable CNT-FET based display technology. © *2011 American Institute of Physics*. [doi:10.1063/1.3524209]

I. INTRODUCTION

The exceptional electronic, thermal, and mechanical properties[1–4] of carbon nanotubes (CNTs) have motivated an extensive study of their use in electronics, energy conversion, and hydrogen storage devices and in thermal interface materials, interconnects, and chemical-biological sensors.[4–16] CNT network based thin-film transistors (TFTs) on flexible substrates have been investigated for large area macroelectronics[13] on plastic or glass substrates to improve performance for applications such as liquid crystal displays (LCDs), e-paper, chem-bio sensors, solar cells and flexible, and shape-conformable antennae and radar.[4,5,7,13,17] High mobility, substrate-neutrality, and low-temperature/low-cost processing make CNT-TFTs very promising for these flexible electronics applications. A number of groups have focused on developing CNT-TFTs for very high performance applications with mobilities reaching up to 1000 $cm^2/V\,s$ using aligned nanotubes, which is comparable to technologies based on single-crystal silicon.[4,18] Fabrication of an integrated digital circuit composed of up to nearly 100 transistors on plastic substrates using random network of CNTs has been reported recently.[9] These developments promise to significantly enhance the performance of the large area macroelectronics. CNT-TFTs are further being explored to substantially increase the performance of flexible electronics to address medium-to-high performance applications in the 10 MHz–1 GHz range.[4]

Present day applications such as LCDs do not require cooling because of relatively low-frequency (~kHZ) of operation. Increasingly though, the interest is in pushing TFT frequencies into the 1–100 MHZ range,[13] and in expanding the range of possible applications. In electronic displays, for example, each pixel is controlled by a small circuit composed of TFTs. Fully transparent and mechanically flexible TFTs based on aligned CNT arrays or a random network of CNTs have been fabricated recently, which demonstrate the potential of these devices for next generation display technologies.[19,20] In transparent display applications, CNT-TFTs are covered by the glass on one side and polymer on the other. The two display surfaces, top and bottom, are usually cooled purely by natural convection. Self-heating is expected to become a severe problem in the high frequency range, especially if active cooling is unacceptable in order to maintain flexibility. If such self-heating severely affects device mobility and diminishes performance, it may limit the commercialization of these devices. It is important to understand the effect of the different thermal resistances in the device on overall thermal transport to predict hot spot temperatures and to explore the requirements of active cooling. This necessitates the development of a coupled electrothermal transport model to analyze the effects of self-heating on

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the device performance and to predict the changes required in design and/or underlying materials to make the technology viable.

Coupled electrothermal transport in *single* CNTs has been explored by the Landauer–Buttiker formalism, Monte Carlo simulations, and Boltzmann transport methods.[21,22] Pop *et al.*[21] analyzed transport in metallic single-wall CNTs on insulating substrates using temperature-dependent Landauer model for electrical transport and diffusive heat conduction for the thermal transport. They used this model to investigate the electrical breakdown of CNTs in air and to estimate the contact resistances between CNTs and the substrate by comparing experimental and computational results. Kuroda and Leburton[22] studied the high-field electrothermal transport in metallic CNTs using a self-consistent model based on the Boltzmann transport equation and the heat equation mediated by the phonon rate equation. Their model reproduces the room-temperature characteristics of metallic CNTs and anticipates the negative differential resistances observed in suspended CNTs.[22] Previous coupled electrothermal modeling approaches however are limited to the analysis of single isolated CNTs. The effect of self-heating in devices based on networks of CNTs has not been explored yet. We have previously developed an electronic transport model for CNT-TFTs using percolation theory and drift-diffusion equations and performed a detailed analysis of the characteristics and performance of CNT-TFTs.[9,23–30] Different regimes of operation of CNT-TFTs based on the CNT network density and Schottky barriers within semiconducting tubes or between semiconducting and metallic tubes have been presented by Topinka *et al.*[31] The present work is a first in building a fully self-consistent electrothermal model to compute the temperature distribution and current-voltage characteristics of network transistors in the high-voltage, nonlinear regimes of transistor operation.

In this paper, we develop a computational model to couple the electrical and thermal transport in CNT network in a self-consistent manner for accurate predictions of both electrical and thermal characteristics. We consider a pixel of electronic display which is controlled by a CNT-TFT for its operation. An electrical-field and temperature-dependent mobility model is used to incorporate the effect of self-heating in the CNT-TFT. We predict the nonuniform spatial temperature distribution in the CNT network and show the effect of three-dimensional electrothermal coupling on device performance and temperature rise as a function of important parameters like channel length, network density, tube-to-substrate thermal conductance, and tube-to-substrate thermal conductivity ratio. Finally, we investigate the effect of active cooling solutions, represented by the heat transfer coefficient, h, in reducing the temperature and enhancing the performance of the device.

II. NUMERICAL MODEL

A. Model for a pixel in an electronic display

As an concrete illustrative example, consider the scenario where the amorphous silicon (a-Si) TFT driving a pixel of a standard laptop display has been replaced by a CNT-TFT [see Fig. 1(a)]. A typical 15 in. display has 1024×768 pixels,[32] which are arranged periodically in the plane of the LCD. Based on these values, the size of a single pixel is approximately $L_P \times L_P = 300 \times 300$ μm^2, which is chosen as the size of our computational domain in the xy plane, Fig. 1(a). A thickness t of 50 nm is chosen in the depth (z) direction normal to the LCD plane. This thickness is chosen as a typical value although a larger thickness will not change the generality and the trends of the results. The display is cooled from the top and bottom z faces. In commercial displays with a-Si TFT matrix, each pixel is controlled by a small circuit of transistors which turns it on and off to get the desired visualization. Nanotube transistors with a high drive current and with better device stability would reduce the number of transistors controlling each pixel. For simplicity, we consider one nanotube transistor per pixel. The TFT is assumed located at the center of the computational domain, as shown in Figs. 1(a) and 1(b), and is typically of size 4×4 μm^2. The TFT consists of a percolating random network of semiconducting nanotubes of length L_t and diameter d randomly dispersed in the midplane of the plastic or glass matrix. Thus the nanotube network is essentially 2D, while the matrix containing it is 3D. Figure 1(a) shows a cross-section of the computational grid with a transistor in the middle. A one dimensional (1D) grid along the CNTs and a 3D grid in the substrate are shown in Fig. 1(c).

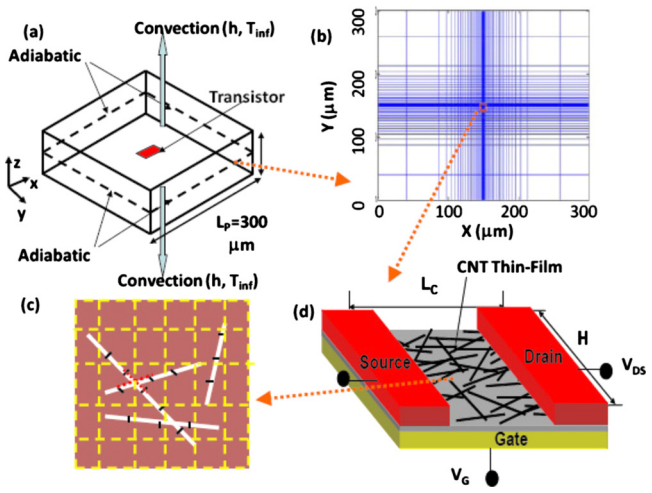

FIG. 1. (Color online) (a) A typical pixel of an electronic display showing the substrate, TFT and boundary surfaces. The size of a single pixel is approximately $L_P \times L_P = 300 \times 300$ μm^2, which is chosen as the size of our computational domain in the (xy) plane. A thickness t of 50 nm is chosen in the depth (z) direction. The lateral boundaries $x=0$, $x=L_P$, $y=0$, and $y=L_P$ are assumed insulated (adiabatic), modeling a periodic arrangement of pixels in the display. On $z=0$ and $z=t$, a convective boundary condition is applied; ambient temperature, $T_{inf}=300$ K). (b) A cross-section of the computational grid showing the transistor in the middle. (c) Schematic of the channel region of the transistor. A 1D grid along the CNTs and a 3D grid in the substrate are shown. (d) A schematic of the TFT made of CNTs; source, drain, gate, and channel region are shown. L_C is channel length and H is width.

We use a coupled electrothermal transport model for analyzing the transport in the pixel geometry with an embedded CNT device described in Fig. 1(a). The thermal dissipation raises the temperature of the device which reduces the electron mobility and hence the drive current of the device.

To solve the thermal transport and electrical transport self-consistently, we first generate a random network of nanotubes of a given density and obtain the electric field and current distribution in the network using the drift-diffusion and Poisson equations (appropriate for transport in the high-bias regime[9,29]). The details of the random network generation for the CNT-TFT model can be found in Ref. 24. For simplicity, we use an electrical-field and temperature-dependent mobility model given by[33]

$$\mu^{-1} = \mu_0^{-1} + v_s^{-1}E; \quad \mu_0 = 12\,000 \ \text{cm}^2/\text{V s} \times (300 \ \text{K/T}) \times (d/1 \ \text{nm})^{2.26}. \tag{1}$$

Here v_s is the saturation velocity and $\boldsymbol{E}$ is the electric field. This expression for the mobility is based on the multiband Boltzmann model presented in Ref. 33. While the temperature and diameter scaling of this theoretical model are consistent with the experimental data,[34] the field-dependence of this mobility model has not been independently validated against experiments. This model also does not include the mobility dependence on charge density. Several recent studies have studied the dependence of mobility on charge density[35] and saturation velocity on electric field[36] and found a complex interplay of scattering, carrier density, and band-structure effects. It would be interesting to incorporate these effects in the current modeling framework. Such dependence and future improvements of the mobility model can be easily incorporated in the numerical simulation framework discussed in this paper. The spatial power in the CNT segments is computed by using $\boldsymbol{P}=\boldsymbol{J}\cdot\boldsymbol{E}$ ($\boldsymbol{J}$ and $\boldsymbol{E}$ are current and electric field vectors), which is in turn used as a Joule heating term for the thermal simulation. Based on the solution of the thermal transport problem, we obtain the temperature distribution in the tube network. We check for the convergence of the results by comparing the present temperature distribution with the temperature distribution from the last iteration. If the convergence is not achieved, we update the electron mobility with the temperature and electric field dependent mobility model of Eq. (1). The device and thermal simulations are performed in an iterative loop at each bias voltage for every ensemble of the CNT network until convergence is achieved (see the loop in Fig. 2), i.e., the norm of the temperature difference between two successive iterations is less than a fixed threshold value (Fig. 2). The details of the electrical and thermal transport model are described in the next two sections. Most of the results reported here are computed by taking an average over 50 random realizations of the network, though more realizations are used for low densities and short-channel lengths. Here, it is assumed that transistor is biased at DC and steady state temperature has been achieved. The analysis can be extended considering the activity level of the transistor which will lead to the reduced temperature (especially at very low frequencies) in comparison to the present analysis.

B. Electrical transport

In the high-bias saturation regime of a transistor, charge density (n) is not constant along the channel of CNT transistor and is dependent on the drain voltage V_D and gate voltage V_G. Therefore, $n\ (V_D, V_G)$ must be determined self-consistently by solving the drift-diffusion equations (appropriate for $L_C > 1\ \mu$m) and the Poisson equation. In the "bottom-up" description of the channel, the drift-diffusion, and Poisson equations are generalized for CNT-TFTs as[28]

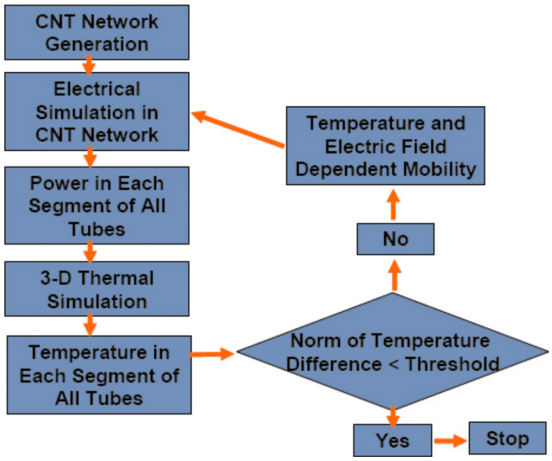

FIG. 2. (Color online) Flow chart for coupled electrothermal modeling. Convergence is achieved when the norm of temperature difference between two successive iterations is less than a fixed tolerance.

$$\left.\begin{aligned} &\frac{d^2\Phi}{ds^2} + \frac{\xi}{\varepsilon} = 0 \\ &\nabla . J_p = 0 \\ &\nabla . J_n = 0 \end{aligned}\right\}$$

$$\sum_{i=1}^{N}\left[\frac{d^2\Phi_i}{ds^2} + \frac{\xi_i}{\varepsilon} - \frac{(\Phi_i - V_G)}{\lambda^2} + \sum_{j\neq i}\frac{(\Phi_j - \Phi_i)}{\lambda_{ij}^2}\right] = 0,$$

$$\rightarrow \sum_i\left[\nabla . J_{pi} + \sum_{j\neq i} C_{ij}^p(p_j - p_i)\right] = 0,$$

$$\sum_i\left[\nabla . J_{ni} + \sum_{j\neq i} C_{ij}^n(n_j - n_i)\right] = 0, \tag{2}$$

where N is total number of CNTs, s is in the direction of individual CNT, ξ is total charge density, and the term $-(\Phi - V_G)/\lambda^2$ (the well known parabolic approximation[37]) introduces the effect of the back gate, where λ is effective screening length with $\lambda^2 = \varepsilon_{\text{CNT}} T_{\text{ox}} d/\varepsilon_{\text{OX}}$. For typical transistor parameters of $d \sim 2$ nm is the thickness of the nanobundle film, $T_{\text{ox}} \sim 250$ nm is thickness of gate oxide, $\varepsilon_{\text{CNT}} \sim 5$ and $\varepsilon_{\text{OX}} \sim 3.9$ are dielectric constants for CNT network and gate oxide,[28] respectively, gives $\lambda \sim 44$ nm. The parabolic approximation is valid in this case because the required condition $L_C \gg \lambda \gg d$ is satisfied.[28] The term $(\Phi_j - \Phi_i)/\lambda_{ij}^2$ is the tube-tube interaction with screening length λ_{ij}, where a node on tube i intersects a node on tube j. The intersecting nodes act as tiny gates for each other modifying the potential and carrier concentrations.[38] Further, transport is essentially 1D (along the tube) with the additional term $C_{ij}^n(n_j - n_i)$ in the continuity equation representing charge transfer between nanotubes at the point of intersection. Here a higher value of $C_{ij}^{n,p} = G_0/G_1$ implies better electrical contact, where G_0 and G_1 is the mutual and self conductances of the tubes.[28] In

general, C_{ij} should reflect the Schottky barriers between metal-semiconducting tubes[31] or even semiconducting tubes of different diameters. Since the present study makes a number of simplifications, including the assumption of semiconducting tubes with a single diameter, we use C_{ij} as an adjustable parameter. Finally, we solve for drift-diffusion and Poisson equations to obtain the current-voltage distribution in the CNT network and the power dissipation in each section of each CNT. This is input to the thermal simulation for the temperature estimations in the device. The detailed description of the electrical transport model can be found in Refs. 28–30.

C. Thermal transport

We use a diffusive modeling framework to simulate the thermal transport in the network of CNT transistor and the pixel matrix (substrate) in which the CNT transistor is embedded. Though microscale heat transfer effects such as phonon ballistic transport and confinement may be important in some regimes,[24] boundary scattering effects are expected to dominate in long tubes, and Fourier conduction may be assumed, albeit with a thermal conductivity that may differ from bulk values. Using the dimensionless variable $\theta=(T-T_{\text{inf}})/(Q'dL_t/k_t)$ for the temperature and nondimensionalizing all lengths by the tube diameter d, the governing equations in the tubes and substrate may be written as[24]

$$\frac{d^2\theta_i}{ds^{*2}} + \sum_{\text{intersecting tubes } j} Bi_c(\theta_j-\theta_i) + Bi_s(\theta_s-\theta_i) + \frac{d}{L_t}\frac{q_i'}{Q'} = 0, \tag{3}$$

$$\nabla^{*2}\theta_s + \sum_{i=1}^{N_{\text{tubes}}} Bi_s\beta_v(\theta_i-\theta_s) = 0, \tag{4}$$

where T_{inf} is the ambient temperature, q_i' is the Joule heating term inside the nanotube with units of power per unit volume and Q' is the reference power per unit volume which is used for nondimensionalizing the temperature term in the heat transport equation. Here, $\theta_i(s^*)$ is the nondimensional temperature of the i^{th} tube at the axial location s^*, and $\theta_s(x^*,y^*,z^*)$ is the substrate temperature. Thermal contact between tubes i and j is characterized by the contact Biot number Bi_C. Heat exchange between each tube and the substrate is governed by the substrate Biot number Bi_S and the empirical contact parameter β.

In Eq. (3), the summation term denotes heat exchange between tube i and all tubes j which have an intersection with it; the term is nonzero only at the point of intersection. Similarly, in Eq. (4), the summation term denotes the volumetric source due to tubes intersecting the substrate. The last term in Eq. (3) corresponds to the Joule heating due to the power dissipation by the electrical current in the nanotube. The dimensionless parameters in these equations are defined as[24]

$$Bi_C = \frac{h_C P_C d^2}{k_t A}; \quad Bi_S = \frac{h_S P_S d^2}{k_t A}; \quad \beta_v = \alpha_v\left(\frac{A}{P_S}\right)\frac{k_t}{k_S},$$

where h_C and h_S are the heat transfer coefficients characterizing tube-to-tube and tube-to-substrate contact, P_C and P_S are the corresponding contact perimeters, k_t is the thermal conductivity of the tube, and A its effective cross-sectional area. The parameter β_v characterizes the contact geometry and α_v is the contact area per unit volume of substrate. Additional dimensionless parameters governing the problem are the conductivity ratio k_S/k_t, tube aspect ratio d/L_t, as well as the geometric ratios L_C/L_t, t/L_t and H/L_t.

The lateral boundaries $x=0$, $x=L_P$, $y=0$, and $y=L_P$ of the pixel are assumed insulated (adiabatic), modeling a periodic arrangement of pixels in the display. On $z=0$ and $z=t$, a convective boundary condition is applied [see Fig. 1(a)]. The convective boundary condition can be expressed as $-k_S dT/dz=h(T-T_{\text{inf}})$, where $T_{\text{inf}}=300$ K is the ambient temperature and h is the heat transfer coefficient between air and the lateral surface of the pixel. In this arrangement, the top and bottom boundaries are expected to be major pathways for heat removal since pixels are arranged periodically in the plane of the LCD and cannot remove heat laterally in a conventional display design. In commercial displays, a glass substrate, the liquid crystal, polarizers, lenses, the front plate, and the outer sealing also provide resistance to heat removal from the top and bottom surfaces. Due to their small thickness, the effective thermal resistance is much smaller than the resistance between outer display surface and the ambient air. In the present model, the resistances of these structures are added to the air resistance to compute an effective heat transfer coefficient, h. All tube tips terminating inside the source, drain or substrate are assumed insulated.

The finite volume method[24] is used to solve the temperature field in the tubes and the substrate. Each tube is divided into 1-D segments, and a control volume balance is performed on each tube segment. Possible contact with other tubes is checked for each segment. Bi_C is zero for the segment if there is no contact. Similarly, the substrate is divided into 3-D control volumes, and a control volume balance is performed. Segments of tubes located in each substrate control volume are identified and their heat exchange is ascribed to the control volume to ensure conservation. The discrete equations for all the tubes and the substrate are solved sequentially and iteratively until convergence. For long channel lengths and large numbers of tubes, the *sequential* solver eventually stalls due to the high degree of coupling between tubes and also between the tubes and substrate. For these situations, a *direct* sparse solver UMFPACK (Ref. 39) is used to solve the resulting system of equations.

III. RANGE OF ELECTRICAL-THERMAL PARAMETERS

Nanotube composites may span a wide range of values of electrical and thermal contact resistances and conductivities. For the present study, good tube-to-tube electrical and thermal contact conductances are assumed; high values for the electrical and thermal contact parameters are considered, i.e., $C_{ij}=10^4$ and $Bi_C=10$ (to establish the lower limits of temperature rise in various applications). The other important

thermal parameters in the present study are k_S/k_t, Bi_C, and Bi_S. The thermal conductivity of free-standing CNTs has been measured at 3000–6000 W/m K,[2,40] though the corresponding values when embedded in a composite are expected to be far smaller due to interface scattering. The thermal conductivity of the substrate is generally low, ranging from 0.1–1.0 W/m K, leading to a wide range in k_S/k_t. For the purposes of this study, we have considered values in the 10^{-1} to 10^{-3} range. The contact parameters Bi_S for tube-substrate contact and Bi_C for tube-tube contact are difficult to determine, and there are few guidelines in the literature to choose them. Experimental studies conducted by Huxtable *et al.*[41] suggest that heat transport in nanotube composites may be limited by exceptionally small interfacial thermal conductance values. The value of the interfacial resistance between the CNT and the substrate was reported to be 8.3 $\times 10^{-8}$ m^2 K/W for CNTs in hydrocarbon (do-decyl sulfate).[41] The nondimensional contact parameter Bi_S evaluated using this contact conductance is O(10^{-5}) assuming the thermal conductivity of a single CNT to be 1000 W/m K. The corresponding values for nanotube-polymer or nanotube-glass interfaces are not known at present. Consequently, values of Bi_S in the range 10^{-2}–10^{-7} were considered in this study. In conventional display designs, the major heat removal is from the top and bottom surfaces of the display. For natural convection in air, the heat transfer coefficient is of order 10 W/m^2 K, while for forced convection in the absence of extended surfaces heat transfer coefficient can be about ten times higher. To analyze the effect of these different convective boundary conditions, the peak temperature rise in tube and substrate is studied for h varying in the range of 10–100 W/m^2 K.

IV. RESULTS AND DISCUSSION

A. Coupled electrothermal transport

We analyze the effect of the self-consistent electrothermal coupling by comparing the device performance and peak temperature rise obtained from a coupled model against an uncoupled model. Here the uncoupled model corresponds to the case when only one iteration is performed in the loop shown in Fig. 2, i.e., device simulation is done just once and temperature is calculated once using the computed Joule heating term in the heat transport equation. The device parameters are $L_C=4$ μm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K. We observe that coupled model predicts a 12% reduction in on-current I_{on} ($V_D=1$ V; $V_G=1.2$ V) compared to the uncoupled model, Fig. 3(a); a device of channel length $L_C=2$ μm is considered. This is due to the reduction in the electron mobility as a consequence of the increased device temperature. For shorter channel length transistors ($L_C=1$ μm), this difference increases to 30%, Fig. 3(a). In general, high I_{on} is expected for shorter channel length devices, which in turn increases power dissipation and temperature rise and leads to a corresponding reduction in transistor mobility. Figure 3(b) shows that coupling reduces peak temperature at the on-state ($V_D=1$ V; $V_G=1.2$ V) by 110 K ($L_C=1$ μm) and 6 K ($L_C=2$ μm), respectively.

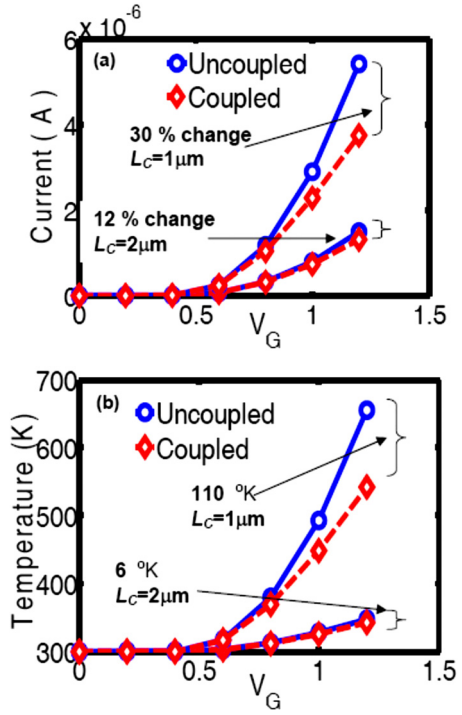

FIG. 3. (Color online) (a) Effect of self-consistent electrothermal coupling. (a) 30% ($L_C=1$ μm) and 12% ($L_C=2$ μm) decrease in I_{on} ($V_D=1$ V; $V_G=1.2$ V) for the coupled model in comparison to the uncoupled model is observed. (b) 110 K ($L_C=1$ μm) and 6 K ($L_C=2$ μm) decrease in peak temperature at the on-state ($V_D=1$ V; $V_G=1.2$ V) for the coupled model in comparison to the uncoupled model is observed. Here, the uncoupled model corresponds to results obtained in a single iteration. $L_C=4$ μm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K.

The power distribution and the corresponding temperature dissipation in a tube network is shown in Figs. 4(a) and 4(b) for the case of $L_C=4$ μm, $L_t=1$ μm, $d=1$ nm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $V_D=1$ V and $V_G=1.2$ V. The ther-

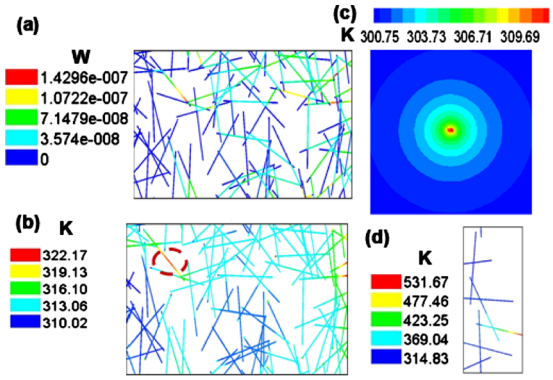

FIG. 4. (Color online) Power distribution in a tube network computed by the coupled solver. $L_C=4$ μm, $L_t=1$ μm, $d=1$ nm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $V_D=1$ V, and $V_G=1.2$ V. CNT segments close to the drain side have high power dissipation in comparison to the source side. (b) Temperature distribution in the CNT network corresponding to Fig. 4(a). A nonuniform spatial temperature distribution is observed with a variation of 12 K. High temperatures in CNT segments close to the drain sides are seen. The tube segment with the highest temperature rise is shown by a dashed elliptical region. (c) Temperature contour plot in the substrate in the plane of the nanotube network. (d) Very high temperature rise in short-channel device ($L_C=1$ μm, $H=2$ μm, $\rho=5.0$ μm^{-2}) shows that tubes may burn for the similar operating conditions. $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K.

mal parameters are $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K. The power distribution plot shows that the power distribution in some tube segments is higher than in others. Consequently, a nonuniform spatial temperature distribution in this typical tube network is observed with a temperature variation in 12 K, Fig. 4(b). High power dissipation and high temperature are observed in CNT segments close to the drain side (hot spot) due to the high electric field, Figs. 4(a) and 4(b). However, some tube segments may have high power dissipation and high temperature rise even though they are located away from the drain region. One such tube segment with highest temperature rise is shown by a dashed elliptical region in Fig. 4(b). A careful consideration of network geometry reveals that this (bridging) segment belongs to a CNT which connects the CNT-cluster located on its left to the CNT-cluster located on its right. Consequently, current flow through such a CNT segment is relatively high, leading to high power dissipation and high temperature rise. In the case of burn out due to self-heating, these CNT segments will burn first, possibly leading to device failure or a significant reduction in the on-current through such devices.

Temperature contour plots in the substrate in the plane of the CNT network show that at a distance of 50 μm from the transistor, the temperature rise is negligible, Fig. 4(c). An excessive temperature rise (>500 K) for short-channel devices ($L_C=1$ μm) suggest that one should be careful about the selection of network density to prevent device burnout, Fig. 4(d). The present analysis of power and temperature distribution will help in selecting an appropriate device length and CNT network density so that burn out may be avoided. In addition, this analysis can be utilized for detecting CNT networks and CNT links which are most prone to burnout.

B. Thermal resistances and conductivities

Tube-to-substrate thermal conductance (Bi_S) and tube to substrate conductivity ratio (k_t/k_S) are influential nondimensional parameters in determining device performance. We analyze the effect of Bi_S and k_t/k_S on on-current of the device (I_{on}), peak tube temperature (T_t) and peak substrate temperature (T_S), Fig. 5. The other parameters are kept constant at $L_C=4$ μm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $h=10$ W/m^2 K, and $T_{inf}=300$ K. Good thermal and electrical contact between tubes is assumed for all simulations. I_{on} increases with increasing Bi_S and increasing k_t/k_S, Fig. 5(a). For low Bi_s, which corresponds to low conductance between tubes and substrate, the temperature rise inside tube is high and this reduces the I_{on} of the device as electron mobility is reduced with increasing temperature, Fig. 5(b). Peak tube temperature (T_t) decreases with increasing Bi_S and increasing k_t/k_S, Fig. 5(b). The opposite trend of I_{on} and T_t with respect to both Bi_S and k_t/k_S can be observed in Figs. 5(a) and 5(b), which is consistent with our temperature-dependent mobility model. Increasing Bi_S or k_t helps in better heat removal from the device, which is reflected in the reduced T_t but enhanced I_{on}. Peak substrate temperature (T_S) increases with increasing Bi_S and increasing k_t/k_S, Fig. 5(c). The change in substrate temperature T_S is dependent on the power dissipation which

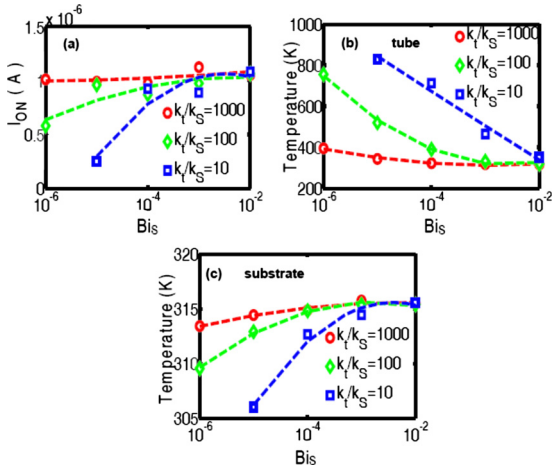

FIG. 5. (Color online) Effect of tube-substrate thermal conductance (Bi_S) and tube-to-substrate thermal conductivity ratio (k_t/k_S). (a) I_{on} ($V_D=1$ V and $V_G=1.2$ V) increases with increasing Bi_S and increasing k_t/k_S. (b) Peak tube temperature (T_t) decreases with increasing Bi_S and increasing k_t/k_S. (c) Peak substrate temperature (T_S) increases with increasing Bi_S and increasing k_t/k_S. The change in T_S follows a trend similar to the change in I_{on} with Bi_S and k_t/k_S. For $Bi_S>10^{-2}$, tube-substrate thermal conductance is not a bottleneck (curves become flat for I_{on}, T_t, and T_S); T_t, and T_S are virtually the same, so that the tube and substrate are in thermal equilibrium. $L_C=4$ μm, $H=2$ μm, $\rho=10.0$ μm^{-2}, $h=10$ W/m^2 K, and $T_{inf}=300$ K.

increases with increasing I_{on}. So, increasing I_{on} or increasing power dissipation with increasing Bi_S and k_t/k_S leads to a corresponding rise in the T_S. This trend is opposite to the trend of tube temperature which decreases with increasing Bi_S and k_t/k_S. The tube and substrate achieve thermal equilibrium for $Bi_S>10^{-2}$, which is reflected in T_t and T_S becoming the same, Figs. 5(b) and 5(c). For high Bi_S values ($>10^{-2}$), Bi_S is not a bottleneck for performance as curves of I_{on}, T_t, and T_S become flat.

C. Channel length and density

Channel length and network density are two dominant parameters to determine the characteristics of the device. We first present the effect of channel length L_C on I_{on} ($V_D=1$ V and $V_G=1.2$ V), T_t, and T_S for $H=2$ μm, $\rho=10.0$ μm^{-2}, $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K, Figs. 6(a) and 6(b). A rapid decrease in I_{on} with increasing channel length L_C is observed but the rate of decrease in I_{on} drops for higher L_C, Fig. 6(a). The corresponding peak temperature in tube and substrate T_t and T_S are shown in Fig. 6(b). At low L_C, device current and hence power dissipation become very high, which is reflected in a very high temperature rise in both tube and substrate. With increasing channel length the difference in tube temperature and substrate temperature decreases substantially. For $L_C>6$ μm, T_t, and T_S are virtually the same, so that the tube and substrate are in thermal equilibrium, Fig. 6(b).

The effect of density on the device performance is presented in Fig. 7(a) for density varying in the range $\rho\sim6.0-12.0$ μm^{-2}. The T_t and T_S dependence on ρ is shown in Fig. 7(b). The other parameters are kept constant at $L_C=4$ μm and 2 μm, $H=2$ μm, $Bi_S=10^{-5}$, $k_t/k_S=1000$, and $h=10$ W/m^2 K. An approximately linear increase in I_{on} and T_t with ρ is observed for the range of network densities con-

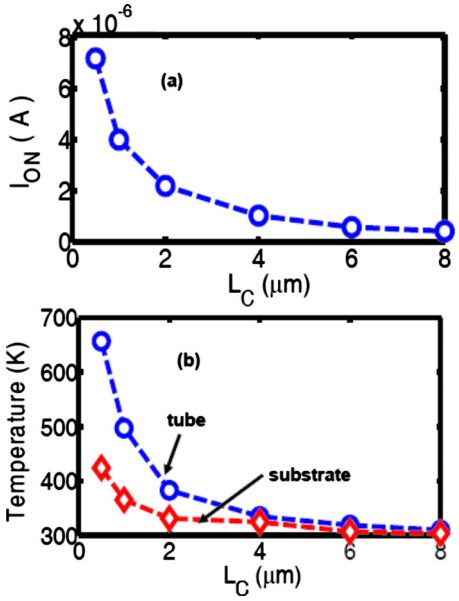

FIG. 6. (Color online) Effect of channel length (L_C). (a) Rapid decrease in I_{on} (V_D=1 V and V_G=1.2 V) with increasing L_C is observed. (b) At low L_C device current power dissipation becomes very high, which is reflected in a very high temperature rise. H=2 μm, ρ=10.0 μm^{-2}, $Bi_S=10^{-5}$, k_t/k_S =1000, and h=10 W/m^2 K.

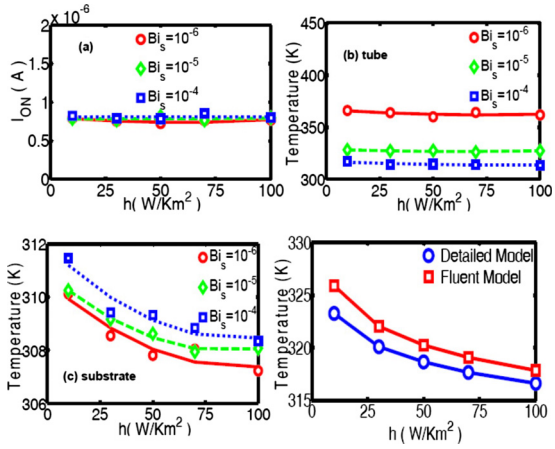

FIG. 8. (Color online) Effect of convective cooling (h). (a) I_{on} is independent of h (10–100 W/m^2 K). (b) T_t decreases with increasing h for h <70 W/m^2 K, but remains independent of h for high h. (c) T_S decreases for h<70 W/m^2 K but remains independent of h for high h. The decrease in T_t and T_S with increasing h is small (~4–5 K) due to the dominance of spreading resistance. (d) Comparison of peak substrate temperature T_S computed by the detailed model against a FLUENT model. A planar source with uniform heat flux at the center of the pixel matrix is applied in the FLUENT model [see Fig. 1(a)]. $Bi_S=10^{-2}$ for the detailed model assuming good thermal contact between the tube and substrate. L_C=4 μm, H=2 μm, ρ =10.0 μm^{-2}, and k_t/k_S=1000.

sidered here for the larger channel length, L_C=4 μm, Fig. 7. I_{on} and T_t have a nonlinear dependence with network density at the lower channel length, L_C=2 μm. Both I_{on} and T_t are very sensitive to the network density and the channel length. While designing a CNT device to control pixel operation one should select an appropriate network density and channel length such that the device temperature does not exceed the acceptable limits. For lower channel lengths, a very high network density may not be acceptable due to temperature constraints, while a large channel length device may be designed with high density of tubes with an additional advantage of reduced fluctuation in device-to-device performance.

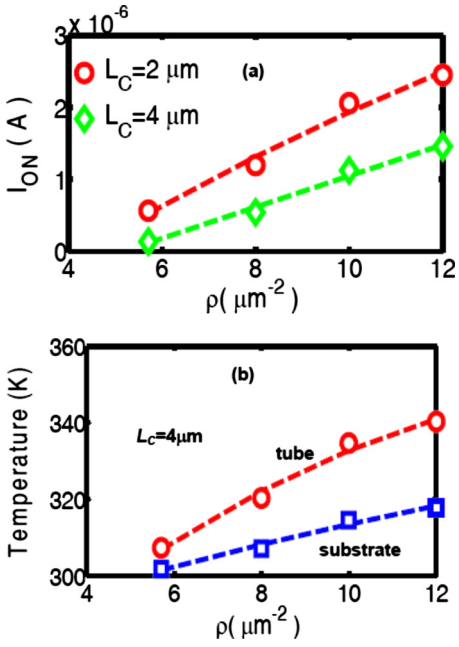

FIG. 7. (Color online) Effect of density (ρ). (a) Linear increase in I_{on} (V_D =1 V and V_G=1.2 V) with density ρ (<12.0 μm^{-2}) is observed. (b) T_t and T_S dependence on ρ are shown. L_C=4 μm, H=2 μm, $Bi_S=10^{-5}$, k_t/k_S =1000, and h=10 W/m^2 K.

D. Technological impact

Let us finally analyze the effect of convective cooling on the performance and temperature rise of the CNT device. The actual numbers for Bi_S and k_t (when CNTs are embedded in a substrate) are not known through the experiments. However, using the experimental values reported by Huxtable *et al.*,[41] $Bi_S \sim 10^{-5}$ for CNTs in hydrocarbon. For this value of Bi_S, and k_t/k_S<500, the peak temperature of device is greater than 500 K, which may lead to device burnout and suggests active cooling may be required, Fig. 5. We consider both natural convection and forced convection cooling on the top and bottom surfaces of the pixel by varying the heat transfer coefficient, h, in the range of 10–100 W/m^2 K. The other parameters are L_C=4 μm, H =2 μm, ρ=10.0 μm^{-2}, and k_t/k_S=1000.

We observe that I_{on} (V_D=1 V and V_G=1.2 V) is independent of h within the limits of statistical error, Fig. 8. T_t and T_S decrease with increasing h for h<70 W/m^2 K, but remain independent of h for high h (>70 W/m^2 K), Fig. 8. In this high-h regime the primary bottleneck to transport is the spreading resistance (R_{SP}) between the transistor and cooling surface at the top and bottom as compared to tube-to-air thermal resistance. The spreading resistance[42] R_{SP} scales approximately as $\sim 1/(4k_S L_C)$ and convective thermal resistance at the pixel surface can be calculated by $1/hA$, where A is the area of the lateral cooling surface. The decrease in T_t and T_S with increasing h is small (~4–5 K) due to the dominance of the spreading resistance. To further validate this dependence of the substrate temperature T_S on h, we develop a diffusive transport model using the commercial

package FLUENT considering a similar pixel of cross-section area, $L_P \times L_P = 300 \times 300\ \mu m^2$, and thickness t of 50 nm in the depth direction [see Fig. 1(a)]. A planar heat source with uniform heat flux at the center of the pixel matrix is applied in the FLUENT (Ref. 43) model to resemble the power dissipation in the CNT transistor. The heat flux on this planar source is computed based on the total power dissipation in the CNT transistor using the detailed model described above. The consideration of uniform heat source in FLUENT model eliminates all physics and unknowns associated with the CNT network model, which helps in analyzing the factors external to the transistor such as spreading resistance. We consider good contact between CNTs and substrate ($Bi_S = 10^{-2}$) in the detailed simulation model of the CNT transistor to resemble the perfect thermal contact between the CNT and substrate in the FLUENT model. The peak T_S of the detailed CNT-pixel model is in good agreement with the FLUENT mode. The temperature predictions are within 2 K by these two different models and trend in T_S with increasing h is very similar, Fig. 8(d). The small difference in prediction of peak T_S between these two models may be due to the assumption of uniform heat flux in the planar source of the FLUENT model. The close agreement between these two models further validate that the spreading resistance is the dominant resistance which diminishes the effect of increasing h in significantly reducing the temperature of the substrate or CNTs.

If forced air cooling were used to increase the value of surface to air heat transfer (high h), *it is likely that the transistor would still remain at a similar temperature*. Decreasing surface to air convective resistance by increasing h may not help in significant reduction in CNT device temperature as the spreading resistance $[R_{SP} \sim 1/(4k_S L_C)]$ may be the dominant component of thermal resistance from device to air. One may have to consider display materials with high thermal conductivity or larger sized transistors in a pixel to reduce the R_{SP} effect or other design modifications need to be employed which can reduce the device to air resistance. Employing distributed liquid microchannels embedded in the display/substrate to cool the high-performance devices may be an option but may be prohibited by cost and manufacturing constraints. The LCDs or other flexible electronics used now a days do not require cooling under normal operating conditions. Maintaining low-cost with flexibility may restrict the use of active cooling in these devices and unless optimized carefully for various applications, self-heating may become bottleneck for the viability of CN-TFT based macroelectronic technology.

V. CONCLUSIONS

In summary, a self-consistent electrothermal model is developed to analyze the transport in a CNT network transistor for electronic display applications. We find thermal dissipation has significant impact on the performance of devices as electron mobility can be significantly reduced. Increasing tube-to-substrate thermal conductance or tube thermal conductivity helps in better heat removal from the device, which is reflected in the reduced tube temperature and enhanced current through the device. An appropriate network density, channel length and width should be selected for CNT-TFTs such that the device temperature does not exceed the acceptable limits. For lower channel length, a very high network density may not be acceptable due to temperature constraints, while a large channel length device may be designed with high density of tubes with an additional advantage of reduced device-to-device fluctuation. The main bottleneck to heat loss lies on the air side for natural convection but spreading resistance due to the substrate plays a role under forced convective conditions. If forced air cooling were used to increase the value of surface to air heat transfer (high h), it is likely that the temperature of the transistor would not decrease much compared to the natural convection value. Better design alternatives need to be explored to prevent burnout of such devices for high performance applications. The present analysis of current, power and temperature distribution in CNT transistors will help in selecting appropriate parameters of CNT network for different applications of CNT-TFTs.

Note added in proof. The present study investigates worst case scenario when transistor is turned on for a long time with relatively low duty cycle. The analysis of transient temperature surge in CNT-TFTs considering frequency of operation and activity level can further provide insights about the limitation posed due to the self-heating.

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