Array of Thermoelectric Coolers for On-Chip Thermal Management

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Site-specific on-demand cooling of hot spots in microprocessors can reduce peak temperature and achieve a more uniform thermal profile on chip, thereby improve chip performance and increase the processor's life time. An array of thermoelectric coolers (TECs) integrated inside an electronic package has the potential to provide such efficient cooling of hot spots on chip. This paper analyzes the potential of using multiple TECs for hot spot cooling to obtain favorable thermal profile on chip in an energy efficient way. Our computational analysis of an electronic package with multiple TECs shows a strong conductive coupling among active TECs during steady-state operation. Transient operation of TECs is capable of driving cold-side temperatures below steady-state values. Our analysis on TEC arrays using current pulses shows that the effect of TEC coupling on transient cooling is weak. Various pulse profiles have been studied to illustrate the effect of shape of current pulse on the operation of TECs considering crucial parameters such as total energy consumed in TECs peak temperature on the chip, temperature overshoot at the hot spot and settling time during pulsed cooling of hot spots. The square root pulse profile is found to be the most effective with maximum cooling and at half the energy expenditure in comparison to a constant current pulse. We analyze the operation of multiple TECs for cooling spatiotemporally varying hot spots. The analysis shows that the transient cooling using high amplitude current pulses is beneficial for short term infrequent hot spots, but high amplitude current pulse cannot be used for very frequent or long lasting hot spots.
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1 Introduction

Power dissipation in microelectronic processors is highly nonuniform on both local and temporal scales which results in several hot spots on chip [1]. Rapid removal of high heat fluxes from these hot spots can provide lower temperatures and greater thermal uniformity on the chip that can significantly improve chip performance and reliability [1–3]. Although conventional cooling technologies involving conduction and convection mechanisms are capable of removing high heat fluxes, they are not able to provide site-specific on-demand cooling of a chip [2]. Design of system level cooling solutions is primarily driven by peak temperatures on the chip. This design approach results in bulky and inefficient cooling systems that are incapable of handling exclusively localized high heat fluxes [3]. Thermoelectric coolers have been proposed as an effective solution for providing site-specific on-demand cooling which may boost the performance of semiconductor devices, improve the reliability of electronic systems, and increase the operation life of electronic circuits [4–7].

Thermoelectric coolers are reliable, long lasting, and noiseless with no moving parts. Despite the operational simplicity of these devices, their fully functional commercial use is often limited due to low efficiency and low heat flux pumping capability. The thermoelectric figure of merit, $ZT = S^2\sigma T/k$, is widely used to compare the performance of different TE materials, where S is Seebeck coefficient, T is absolute temperature and σ and k are the electrical and thermal conductivities, respectively [8]. Significant efforts have been made in recent years to improve ZT by investigating a wide range of alloys and super-lattices of different materials such as SiGe, Bi_2Te_3, Sb_2Te_3 and skutterudites [4,9–11]. The additional challenges for commercial usage of TECs in electronics cooling applications are low heat flux pumping capacity and fully functional and practical integration with electronic devices [2].

The size of the thermoelectric pellets in a thermoelectric module (TEM) affects the overall size of the device and therefore influences the feasibility of integrating TECs within an electronic package. Pellet geometry also has significant effects on the TEC performance and crucial operating parameters such as cooling rate, coefficient of performance, temperature difference across the TEM, and operating current and voltage [12]. A limiting factor of the TECs with small thermoelectric pellets is the interfacial resistances as they become a bottleneck in performance as size of the pellets decreases [12]. Interfacial resistances have a large impact on design and implementation of thermoelectric coolers. The thermal and electrical contact resistances at the TEC's interfaces are affected by the fabrication process and are considered as the most critical parameters affecting the device performance [13]. High electrical and thermal contact resistances significantly degrade the performances of these devices [14,15].

TECs can be utilized both for steady as well as transient operations. Their steady state behavior is well studied and utilized in various commercial applications [16]. Pulsed operation of TECs can provide additional cooling over steady state for a short period of time [17–19]. The Peltier effect appears at the junction of thermoelectric elements while Joule heating occurs throughout the volume of the thermoelectric elements. This difference, between surface effects and volume effects, explains the additional cooling during transient pulsed operation, i.e., Peltier cooling occurs before the effect of Joule heating is realized at the cold junction. This transient behavior has been studied in detail theoretically and experimentally by Snyder et al. [17]. In

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this study, they explored various parameters such as current pulse amplitude, thermal diffusivity, super-cooled temperature and time to reach minimum temperature; the study was focused on thick TEC modules. Transient TEC operation was also studied in shape memory alloy actuators and it was found that the pumping of heat to and from the shape memory alloy produces an actuation force [20,21].

Phase change materials (PCMs) are also considered as potential candidate for transient hot-spot cooling. PCMs act as a heat storage unit during power surges, which helps in suppressing the transient junction temperature rise on the chip, but applications of PCMs are limited to relatively short power surges and long periods of time between power surges [22]. PCMs need recovery time to release the stored heat before the next power surge. If the PCM has not been given this recovery time, the material can fully change phase and is no longer helpful for controlling the temperature rise. Phase change materials are a passive source of cooling and are thus more difficult to control and do not have a mechanism for shutting off if the PCM begins to hurt the system's performance. Thermoelectric coolers on the other hand are an active source of cooling that can be controlled easily by adjusting the input current and can be shut off if the TEC begins to hurt the system's performance. Both cooling solutions are currently being researched for integration inside microchip packaging.

Chip-scale integration requires ultrathin TEC modules where electrical and thermal contact resistances at the super-lattice-metal interface and the TEC module-spreader interface can affect the TEC performance [2]. Some efforts have been made to study the effect of these parasitic resistances and it has been suggested that the impact of contact resistance can be much more pronounced for thermoelectric coolers of length of the order of 100 μm or smaller [14,15,23]. Wang et al. have studied the effects of various crucial contact parameters such as electrical contact resistance on the performance of silicon based thermoelectric microcoolers. Their study employed an analytical model to explore the effect of electrical contact resistance and the width of the lead used to send current into the microcooler. They report that electrical contact resistance could potentially degrade the TEC performance up to 43% [23]. Pulse cooling performance is severely degraded by Joule heating due to these parasitic contact resistances [15].

Recently, TEC modules made of ultrathin ($\sim$100 micron) Bi_2Te_3 based super-lattices have been successfully integrated to the heat spreader of the electronic package with total cooling up to 15 °C at the hot spot [2]. This suggests the possibility of cooling dynamic hot spots by integrating multiple thermoelectric coolers that can be switched on and off on demand at the location of dynamic hot spots. An on-chip array of multiple thermoelectric coolers has been fabricated by Goncalves et al. [24]. The authors have observed a maximum temperature difference of 5 °C between hot and cold sides of TEC. The cooling effects of their TECs were degraded by high electrical resistance and low thermal conductance at the interface of the thermoelectric material [24]. Our previous work develops a model for a single TEC integrated with an electronic package and correlates the important characteristics of transient thermal behavior of hot spot under the TEC operation with crucial thermal and electrical contact resistances inside a TEC module and the properties of the thermoelectric materials [25].

In a typical electronic package, the hot spots can be time and spatial varying which requires multiple TECs to be integrated inside a package and controlled independently. The conductive coupling of these TECs can significantly affect both steady-state and transient operation of TECs. During transient operation, current pulse shapes need to be carefully considered in order to minimize the energy consumption in Peltier cooling. A study of conductive coupling and pulsed cooling in the context of multiple ultra-thin TEC modules on the active side of electronic package has not been performed before.

Our ultimate goal is to develop an integrated framework which can help in investigation and design of controlled and efficient operation of multiples TECs in cooling spatial and time varying hot spots on a micro-processor chip. As a step towards this goal, this paper develops a detailed 3D thermal model of the electronic package with multiple integrated TECs to investigate the effect of steady state and transient operation of TECs on hot spot temperature reduction. Our numerical model incorporates the effect of Peltier cooling and Joule heating, due to the volumetric and contact resistances inside the TEC module, to analyze the temperature reduction at hot spots on the chip. The developed model investigates the effect of conductive coupling among active TECs in hot spot cooling for currents of different magnitudes and shapes. We investigate energy consumption during TEC operation which helps in evaluating the various pulse shapes. We provide a basic set of metrics by which one can judge different methods of pulsing the TECs. At last, a simple control scheme is tested to control temperature on a chip with random hot spots.

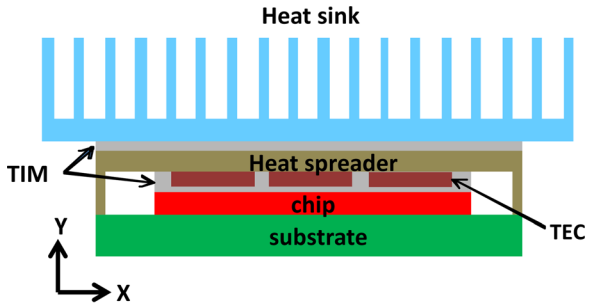
The rest of the paper is organized as follows: Sec. 2 explains the governing equations for the TEC operation, and the developed computational model. In Sec. 3, the conductive coupling among TECs is investigated for both steady-state and transient operation. Sec. 4 studies the Peltier cooling behavior while using transient pulses of different amplitudes, shapes and duration. In Sec. 5, the various pulse shapes are compared using a simple set of metrics and a control scheme is tested to control temperature of dynamic hot spots. Finally, Sec. 6 concludes the paper.

2 Computational Methodology

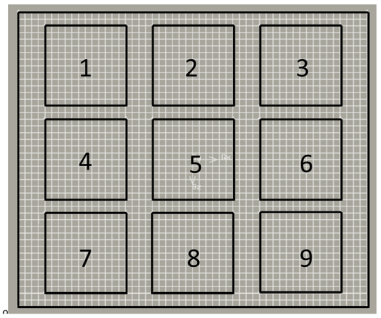
We develop a computational model to analyze the effect of a TEC device on the temperature reduction at a hot spot on chip. The developed model solves Fourier's conduction equation in the electronic package and TEC module to obtain temperature distribution. A schematic of the electronic package including the TEC modules and heat sink is shown in Fig. 1(*a*). We consider nine TEC modules each 100 μm thick and comprised of 7×7 p-n couples; these modules are attached at the back side of the heat spreader. The area of each TEC device is considered to be 3 mm $\times$ 3 mm. The thickness of the superlattice material in a TEC device is 8 μm [2] which is sandwiched between two metallic layers. We have selected this geometry to compare and validate our modeling results against the steady-state experimental and computational results presented in Ref. [2]. The details of the validation can be found in our previous work on Peltier cooling [25]. The reference values of electrical/thermal contact resistances at the interface of superlattice-metal layer (10^{-11} Ωm^2; 1×10^{-6} m^2 K/W) and of thermal contact resistance at the interface of TEC module-heat spreader layer (8×10^{-6} m^2 K/W) are also taken from Ref. [2]. These values of contact resistances are considered in all simulations unless stated differently. Dimensions and thermal conductivity of different components of the electronic package and TEC module are listed in Table 1.

Our computational domain includes heat spreader, thermal interface material (TIM), chip, and nine thermoelectric coolers (TECs). The layout of nine TECs and the associated mesh is shown in Fig. 1(*b*). To reduce the computational time of the simulation, the heat sink is represented by convective heat transfer boundary condition ($h = 2{,}050$ W/m^2-K) at the top of the spreader surface. Nine high heat flux (1000 W/cm^2) sources are located at the bottom surface of chip (each with area 500×500 μm^2) to generate hot-spots at the corresponding locations. Each of the nine high heat flux sources lies at the center of nine TECs. The rest of the bottom surface is considered as heat source of uniform heat flux of 43 W/cm^2.

The operation of TECs is based on the interplay of Peltier cooling and Joule heating. Heat is absorbed at one side of the TEC module (cold-junction) and rejected at the other side of the module (hotter junction) when a TEC module is turned on. We incorporate the Peltier cooling effect by adding heat ($\sim SIT_h$) at the



(a)



(b)

Fig. 1 (*a*) Schematic of an electronic package. Heat spreader, thermal interface material (TIM), chip, substrate and thermoelectric coolers (TECs) are shown. (*b*) Layout of nine TECs and the associated mesh in a 2D cross-section.

hotter side and subtracting heat ($\sim SIT_c$) from the colder side of the super-lattice structures. Here, T_h and T_c are the temperatures of the hotter and colder junctions. The value of S is taken as 300 μV/K based on the experimental measurement in Ref. [2]. The volumetric heat generation inside the TE layer and at the interface of the super-lattice/metal layer and the TEC module/heat spreader layer is considered by adding joule heating ($\sim I^2R$) terms at the corresponding layers and volumes. The thermal contact resistances at these interfaces are incorporated by adding an appropriate thermal resistance at the corresponding interfaces.

2.1 Governing Equations. The governing differential equation for heat distribution inside the electronic package is represented as,

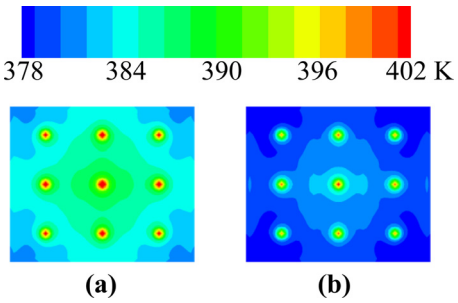
$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}+\dot{Q}=\frac{dT}{\alpha dt} \tag{1}$$

$$\text{where } \dot{Q}=\begin{Bmatrix}\frac{I^2}{A^2\sigma k} & \text{inside TEC}\\ 0 & \text{elsewhere}\end{Bmatrix} \tag{2}$$

Here, T is temperature, α is thermal diffusivity, I is current, A is area of an element, σ is electrical conductivity and k is thermal conductivity.

Table 1 Dimensions and thermal conductivity of different components of the electronic package

Component	Thermal Conductivity (W/m-K)	Dimensions
Spreader	400	30 mm × 1 mm × 30 mm
TIM	1.75	11 mm × 0.125 mm × 13 mm
TEC-superlattice	1.2	3.0 mm × 0.008 mm × 3.0 mm
Chip	140	11 mm × 0.5 mm × 13 mm



(a) (b)

Fig. 2 (*a*) Temperature contours on the bottom surface of the chip with no TECs turned on. High heat flux (1000 W/cm^2) sources are located at nine symmetrical points of area 500 × 500 μm^2 which generate hot-spots. The rest of the surface has a uniform heat flux of 43 W/cm^2. (*b*) Temperature contours on the bottom surface of the chip with TECs turned on at 1.5 amperes.

2.2 Boundary Conditions. A heat flux boundary condition is applied at the bottom of the chip, which can be expressed as:

$$-k\frac{\partial T}{\partial y}=q'' \text{ where } q''=\begin{Bmatrix}1,000\ W/cm^2 & \text{at the hot spot}\\ 43\ W/cm^2 & \text{elsewhere}\end{Bmatrix} \tag{3}$$

In addition, at the cold end of TEC,

$$-kA\frac{\delta T}{\delta y}\Big|_{y=y_c^+}=\left[-kA\frac{\delta T}{\delta y}-SIT\right]_{y=y_c^-}+I^2R_{elec} \tag{4}$$

Here, the y coordinate is directed from TEC to the heat spreader, and y_c^+ and y_c^- are locations just above and below the cold junction. S is Seebeck coefficient and R_{elec} is contact electrical resistance.

Also, at the hot end of the TEC,

$$-kA\frac{\delta T}{\delta y}\Big|_{y=y_h^+}=\left[-kA\frac{\delta T}{\delta y}+SIT\right]_{y=y_h^-}+I^2R_{elec} \tag{5}$$

where y_h^+ and y_h^- are locations just above and below hot junction.

Finally, at the top surface of heat spreader,

$$-k\frac{\delta T}{\delta y}=h(T-T_\infty) \tag{6}$$

where h is convective heat transfer coefficient and T_∞ is ambient air temperature, which is taken as 300 K.

The simulations are performed using the finite volume method based commercial solver FLUENT. We consider 250 K cells for the simulations; grid independence tests verify that these cells are sufficient for the further simulations. Temperature contours on the chip bottom surface of the electronic package with and without TECs is shown in Fig. 2.

3 Effect of Conductive Coupling Among Multiple TECs

In this section, we first analyze the simultaneous operation of multiple TECs and investigate the effect of conductive coupling among active TECs in cooling multiple hot spots on the chip. This is followed by the transient analysis of cooling multiple hot spots using pulsed currents in TECs.

3.1 Steady-State Analysis. The primary purpose of developing a model with nine hotspots and TECs is to investigate the conductive coupling between TECs and the advantages or disadvantages of having multiple TECs inside a package. Simulations were performed for four different cases to investigate the effects of nine TECs (Fig. 1) on steady-state cooling of hot spots.

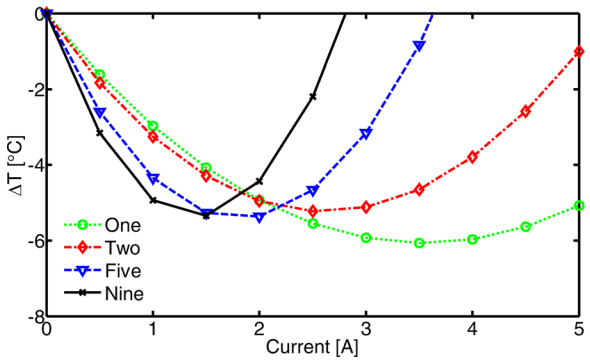


Fig. 3 Temperature change at the center hot spot (ΔT) for various configurations of active hot spots and TECs: (1) Only center hot spot active, (2) Hot spots 5 and 6 active, (3) Hot spots 2, 4, 5, 6, and 8 active, (4) All nine hot spots active

Hot spots with high heat flux sources (1000 W/cm^2) are turned on at specific locations on chip while a uniform low heat flux (43 W/cm^2) is applied to the rest of the chip. In case 1, only one hot spot at the center and corresponding TEC (at location 5 in Fig. 1(*b*)) are turned on. In case 2, two adjacent hot spots and corresponding TECs (locations 5 and 6) are turned on. In case 3, five hot spots and corresponding TECs (locations 2, 4, 5, 6, and 8) are turned on. In case 4, all nine hot spots and TECs are turned on. Case 1 tests the cooling of a single hot spot on the chip whereas cases 2, 3, and 4, test the conductive coupling of active TECs located next to each other in different arrangements. The temperature change at the center hot spot (ΔT) for these various cases are shown in Fig. 3. Two important features of the conductive coupling between TECs can be observed: (i) the maximum cooling (ΔT_{max}) occurs at higher amplitude currents when fewer hot spots and TECs are turned on or active, and (ii) ΔT_{max} is better for a single TEC and hotspot than the other cases which have multiple hot spots and TECs. The maximum cooling for Case 1 is 6 °C at a current of 3.5 amperes (∼optimum current). Case 2, corresponding to the adjacent positioning of a second active TEC, have relatively similar cooling behavior with the maximum cooling of 5 °C occurring at 2.5 amperes current. When five hot spots and TECs are turned on, the maximum cooling (∼ 5.4 °C) occurs at 2 amperes. For case 4, where all nine hot spots and all nine TECs are turned on, the maximum cooling occurred at 1.5 amperes with 5.3 °C of cooling. As the number of hot spots increases from one to nine, ΔT_{max} decreases; however, the decrease in ΔT_{max} is very small as it varies by only 1 °C.

It is important to understand the behavior in Fig. 3 due to the conducting coupling of active TECs. The temperature along the centerline of the bottom of chip for one active TEC (Case-1), five active TECs (Case-3), and nine active TECs (Case-4) are shown in Fig. 4(*a*) with and without associated TECs turned on at each configuration's optimal current. As seen, more hotspots result in higher temperatures across the chip, but the TECs are capable of lowering temperatures uniformly across the chip. However, the temperature gradients across the chip are very high even with active TECs; this suggests that smaller size TECs may be better to cool localized hot spots and simultaneously mitigate the temperature gradient across the chip. The total heat passing through the cold side of the center TEC [Q_{in} (Watts)] and the maximum cooling [in °C] at center hot spot location for 1, 5, and 9 active hotspots and active TECs are shown in Fig. 4(*b*). Turning on an additional hot spot leads to a 2.5 W increase in the chip total power dissipation. The Q_{in} through the center TEC decreases from 9.6 W to 7.4 W from the case of one active hot spot to nine active hot spots and ΔT_{max} also decreases from 6 °C to 5.3 °C. This 23% decrease in Q_{in} suggests that once adjacent TECs are active, they pump out heat from the chip and decrease the cooling load (∼Q_{in}) placed on the center TEC. Figure 5 shows the temperature distributions, 10 μm below the chip-TIM interface, when only the center hotspot and center TEC are turned on at 2 amperes (Fig. 5(*a*)) and when center hotspot, center TEC and two adjacent TECs are turned on at 2 amperes (Fig. 5(*b*)). The temperature contours clearly show that active TECs adjacent to the center TEC create a large temperature gradient (∼10 °C) and pull heat from the center as shown by the arrows in Fig. 5(*b*). We also perform simulations with active hot spots adjacent to the center hot spot but adjacent TECs in off state. It has been observed that in this case ΔT_{max} increases with increasing number of hot spots or increasing power on the chip, but when adjacent TECs are also active ΔT_{max} decreases. The decline in cooling at center hot spot could be due to the additional Joule heating when TECs adjacent to

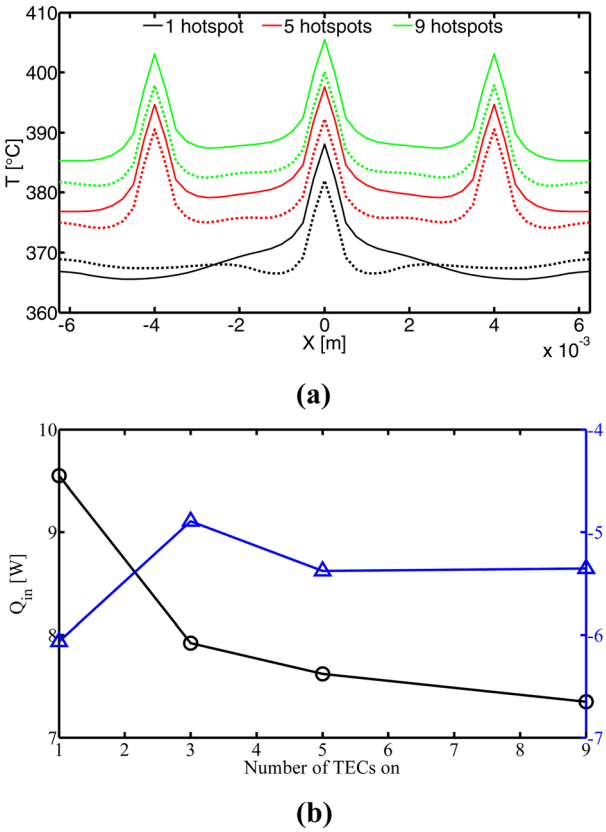


Fig. 4 (*a*) Centerline temperatures for 1, 5, and 9 hotspots turned on; solid line is with no TEC, and dashed line is with TEC turned on with optimal steady-state current. (*b*) Heat passing through the cold side of the center TEC (Q_{in} in Watts) and maximum cooling (°C) at the center hot spot when 1, 3, 5, or 9 hotspots with corresponding TECs turned on with optimal steady-state current (see Fig. 3 for optimal current).

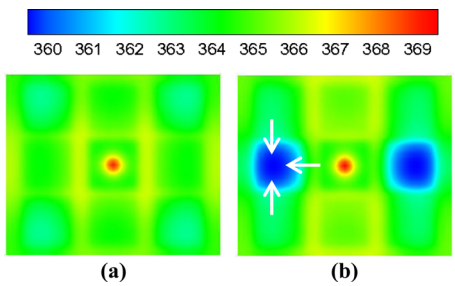
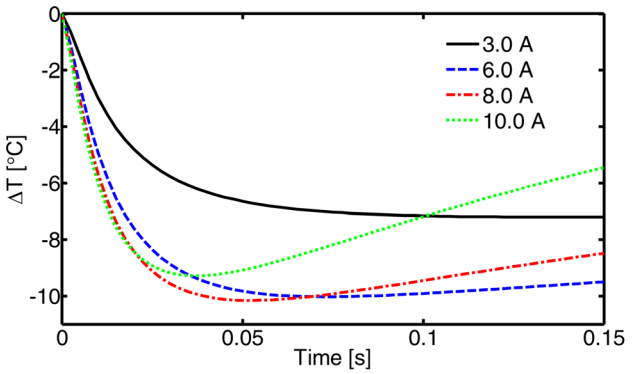
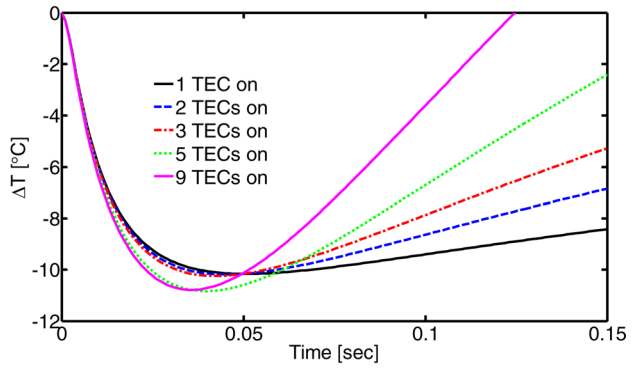


Fig. 5 Temperature contours in a horizontal cross-section of chip at 10 μm below the chip-TIM interface when only center hotspot is active. (*a*) center TEC turned on at 2 amperes, and (*b*) center and two adjacent TECs turned on at 2 amperes; arrow shows heat flow direction due to the active TEC at left side.



(a)



(b)

Fig. 6 (*a*) Transient analysis of a single hot spot; TEC turned on with 3.0 A, 6.0 A, 8.0 A, and 10.0 A current; (*b*) Transient analysis with 8.0 A current for various number of hotspots and active TECs

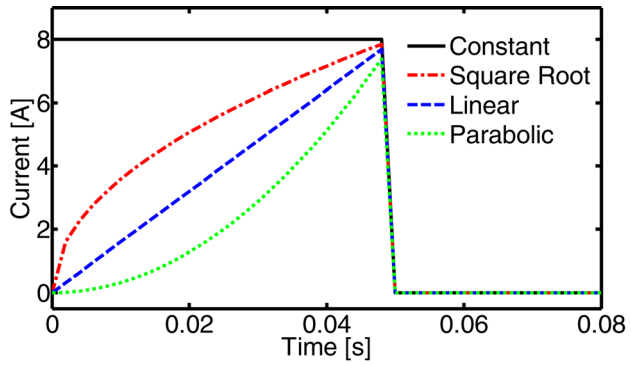
the center TEC become active. The Joule heating through the adjacent TECs also leads to a decrease in the optimal current through the center TEC (Fig. 3). However, the overall effect is optimistic as even at lower selected currents, the decrease in ΔT_{max} is very minimal, suggesting that multiple TECs can be employed for localized cooling. The conductive coupling between TECs can be very strong especially when Joule heating in one TEC device can significantly affect the operation of adjacent TECs; careful design and control is required for energy efficient operation of such multiple TECs.

3.2 Transient Analysis. Transient current pulses through the TECs can lead to additional cooling above Peltier cooling in steady-state operation [17–19]. Selection of these current pulses can lead to efficient on-demand cooling of hot spots in microelectronic chips. It is important to analyze the effects of conductive coupling of TECs on the transient operation as these effects may be significantly different from the steady-state results due to the large variation in thermal capacitances of the different materials inside an electronic package. Figure 6(*a*) shows the results of a transient analysis with a single hot spot turned on till steady state is reached, and then the corresponding TEC is turned on with a step current pulse of amplitude in the range of 3.0–10.0 amperes. The results corresponding to 3.0 amperes show that the temperature is monotonically decreasing and ΔT is approaching the steady-state values after 0.1 s. Higher amplitude pulse current through the TEC results in higher ΔT, but for higher amplitude current pulses the cooling effects disappear with time as the effect of Joule heating in TEC is realized at hot spot on chip. As seen for the case of 10.0 amperes applied current, the cooling is approximately 9.0 °C at 0.03 s but decreases to 7 C by 0.1 s which is worse than the corresponding cooling by 3.0 amperes applied current. The best transient cooling of 10 °C occurred for a current of 8.0 amperes and duration of 0.05 s. These results were used as the guidelines for the pulse shapes used in the following transient simulations. The 8.0 A current amplitude is selected for the following analysis and the number of active hotspots and TECs were varied from one to nine. The transient temperature change (ΔT) of the center hotspot is presented in Fig. 6(*b*). The maximum ΔT and time to reach maximum ΔT (ΔT_{max}) is similar for the cases of one, two or three hot spots and active TECs at the corresponding locations. The ΔT_{max} increases by approximately 1 °C at the center hot spot as the number of TECs and hotspots increase to nine and the time to reach ΔT_{max} decreases from approximately 0.05 s to 0.03 s. This analysis shows that the transient coupling between TECs are much weaker compared to the steady-state coupling. However, it should be noticed that the trajectory of temperature rise is very different for these different cases of active TECs after the time to reach ΔT_{max}. This means that if the TEC at a hot spot needs to be turned on before the system reaches steady state after turning off an adjacent TEC, then coupling effects can be stronger and need to be considered. Some of these effects can be observed in Sec. 5.2 for random hot spot temperature control.

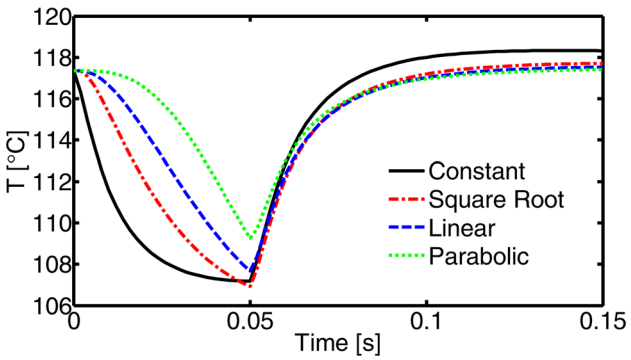
4 Pulse Shape and Duration

Shape of the current pulse can significantly affect the maximum cooling, energy consumption, and post-pulse behavior at the hot spot location. In this section, various pulse shapes were investigated to analyze and compare them for hot spot temperature management. The best pulse obtained from the analysis will be used to analyze the temperature control in the next section. The pulses under investigation are a step pulse (t^0) of constant amplitude of 8 amperes and pulses whose magnitude increases from 0 amperes to 8 amperes along linear (t), square root ($t^{0.5}$), and parabolic paths (t^2) [26]. Figure 7(*a*) shows the pulse shapes used in the transient simulations. For the study of transient pulse simulations, only the center hot spot is turned on and different pulses are applied to the corresponding TEC only (location 5). The system is first allowed to reach steady-state with the hot spot turned on and no current passing through the TEC. After reaching steady state, current pulses of different shapes were applied to the TEC to analyze hot spot cooling. The transient change in hot spot temperature corresponding to different pulses is presented in Fig. 7(*b*). The best cooling at the hot spot is obtained by using square root pulse ($\sim \Delta T_{max} = 10.4$ °C). A similar degree of cooling ($\Delta T_{max} = 10.2$ °C) is also obtained by using step pulse or constant amplitude pulse, but the temperature overshoot after turning off the pulse is higher compared to other pulses; we also observe that this pulse consumes maximum energy (see next section) even though it leads to fastest cooling over the period of the pulse (Fig. 7(*b*)). Linear and parabolic pulses cool the hot spot by 9.7 °C and 8.1 °C, respectively.

A subsequent study is performed to investigate the effect of the pulse period. We select the best pulse shape observed from the above analysis, i.e., square root shaped pulse with maximum amplitude of 8 amps. The time length or period of the pulse is varied in the range of 2.5 ms to 15 ms. Similar to the previous analysis, the chip is allowed to first reach steady-state with the center hot spot turned on and the TEC is then turned on with the square root pulses of various time lengths. As observed in Fig. 8, the maximum hot spot cooling by TEC increases up to 10 ms pulse and then begins to decrease for longer pulses. This suggests that there should be an optimal pulse length corresponding to maximum cooling for any shape of pulse of given maximum amplitude. This analysis provides a very important suggestion about the hot spot cooling, i.e., if transient cooling for a longer time is required, then longer duration pulses of same maximum amplitude can help but with a compromise in maximum degree of cooling at the hot spot. The longer duration pulse can provide extended cooling, but once the pulse is turned off the temperature increases rapidly leading to larger temperature overshoot with increasing pulse period.



(a)



(b)

Fig. 7 (*a*) Pulse shapes used in transient analysis include constant, linear, square root, and parabolic; (*b*) Hot spot 5 turned on with a high heat flux of 1000 W/cm^2 and allowed to reach steady-state; TEC turns on with various pulses: constant, linear, root, and parabolic

5 Temperature Control and Energy Analysis

In a microelectronic package, the TEC will be activated based on a threshold temperature sensed on the chip. In this section, we analyze a single hot spot control and random hot spot control by TECs once hot spot temperature crosses a specified temperature threshold. Pulse shapes analyzed in the previous sections are further used for hot spot temperature control and investigation of energy consumption during the TEC operation.

5.1 Temperature Control of Single Hot Spot. Each pulse shape have different cooling behavior and thus a metric is required for comparing different pulse shapes used for removing a transient heat flux. Energy consumption coupled with the degree of cooling at a hot spot for different pulses can provide an elementary set of guidelines to judge the application of an appropriate pulse to a TEC. In addition, some important factors need to be considered to select an appropriate pulse such as the maximum temperature overshoot after the pulse is turned off, and the time the system takes to reach steady-state again. The next set of simulations is performed to evaluate the pulse shapes studied in the previous section using the important parameters discussed above. The system is first allowed to reach steady-state with no hot spots turned on and no TECs turned on. The center hot spot is then turned on and once the temperature of the hot spot reaches a preselected threshold of 102 °C, the corresponding TEC is turned on using the pulses shown in Fig. 7. The pulse duration is considered same to the lifetime of the transient heat flux, i.e., 0.05 s. Among four current pulses, the constant pulse provides the fastest cooling of 10 °C, Fig. 9. Here, the degree of cooling is estimated at the end of the pulsed operation with a reference to the peak temperature (∼115 °C) in the absence of any pulsed current through the

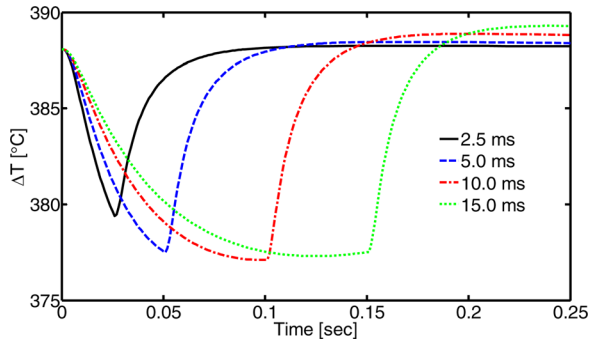
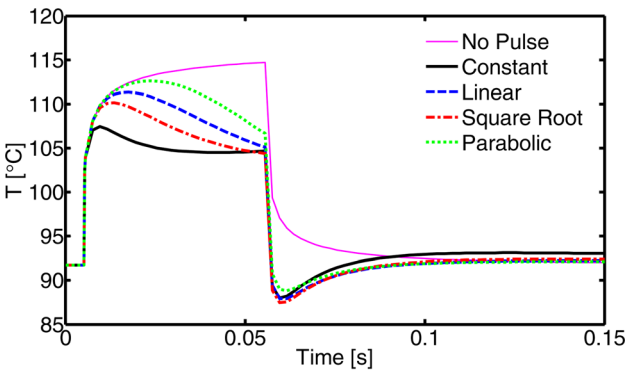


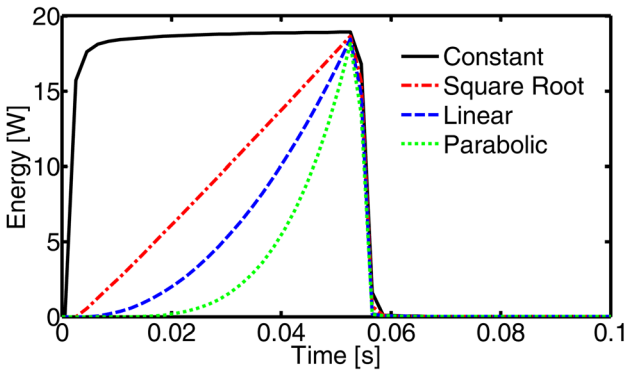
Fig. 8 Hot spot 5 turned on with a high heat flux of 1000 W/cm^2 and allowed to reach steady-state; TEC turns on with square root pulse of various periods: 2.5 ms, 5.0 ms, 10.0 ms, 15.0 ms

TEC, Fig. 9. The square root pulse responds slower than the constant pulse but gives the best cooling of 10.5 °C. The linear and parabolic pulses provide relatively slower cooling than the constant and square root pulses with cooling of 9.9 °C and 8.6 °C, respectively.

Analysis of total energy consumed during the pulsed operation can be used to determine which pulse is most energy efficient. Figure 9(*b*) shows the energy consumed over time, which is then integrated to find the total energy consumed for each pulse as shown in Table 2. The constant pulse consumes 204.9 J, approximately twice the energy required by the square root pulse, which uses 103.2 J. The linear and parabolic pulses use 70.8 J and 45.1 J, respectively. Even though the parabolic shaped pulse is best from the energy perspective, it is slowest in response and less



(a)



(b)

Fig. 9 Hot spot 5 turns on with a high heat flux of 1000 W/cm^2 and TEC turns on at 102 °C for various pulses: constant, linear, root and parabolic; (*a*) Actual temperatures of simulations, (*b*) Energy consumed over time

Table 2 Total energy expended for cooling of hot spot using four pulse shapes: (1) constant, (2) linear, (3) root, and (4) parabolic

Pulse Shape	Total Energy Expended (Joules)
Constant	204.9 (100%)
Linear	70.8 (34.6%)
Square Root	103.2 (50.4%)
Parabolic	45.1 (22.0%)

effective in controlling the temperature of the hot spot. The square root pulse seems to be the winner here as it has same degree of cooling but at half the energy expense of the constant pulse.

Other factors which need to be considered include highest temperature, maximum temperature overshoot after the pulse is turned off, and the time the system takes to reach steady-state. These statistics are compared for each pulse in Fig. 10. The pulses are displayed as follows: (1) Constant, (2) Linear, (3) Root and (4) Parabolic. Figure 10(*a*) shows the difference (ΔT) between the maximum temperature and the threshold temperature ($\sim$102 °C) that triggers the pulse. The constant pulse has the best ΔT of 5.7 °C followed by the square root pulse with 8.1 °C. The linear and parabolic pulses have ΔT's of 9.3 °C and 10.6 °C, respectively. Figure 10(*b*) shows the temperature overshoot (ΔT_{sh}), which is defined as the difference between the maximum temperature after the pulse and hot spot are turned off and the steady-state temperature. The parabolic pulse has the best overshoot with 0.4 °C, followed by the linear pulse at 0.5 °C. The square root pulse and constant pulse have ΔT_{sh}'s of 0.7 °C and 1.4 °C, respectively. Figure 10(*c*) compares the total energy consumed during pulsed operation discussed in Table 2. Figure 10(*d*) shows the settling time for each pulse, which is defined as the time when hot spot temperature is within 0.5 degrees of the steady-state temperature after the pulse and hot spot are turned off. Settling time provides a metric to quantify the duration of adverse Joule heating effects of a current pulse after the pulse is switched off. The constant pulse takes the longest settling time of 0.5 s. The square root pulse is second longest at 0.25 s, but it takes considerably less time than the constant pulse. The linear pulse and parabolic pulse are the best with times of 0.16 and 0.08 s, respectively. Comparing pulses based on the combination of these four factors suggest that square root pulse is the best pulse of all pulse shapes tested; it is used for further testing the system with random hot spots.

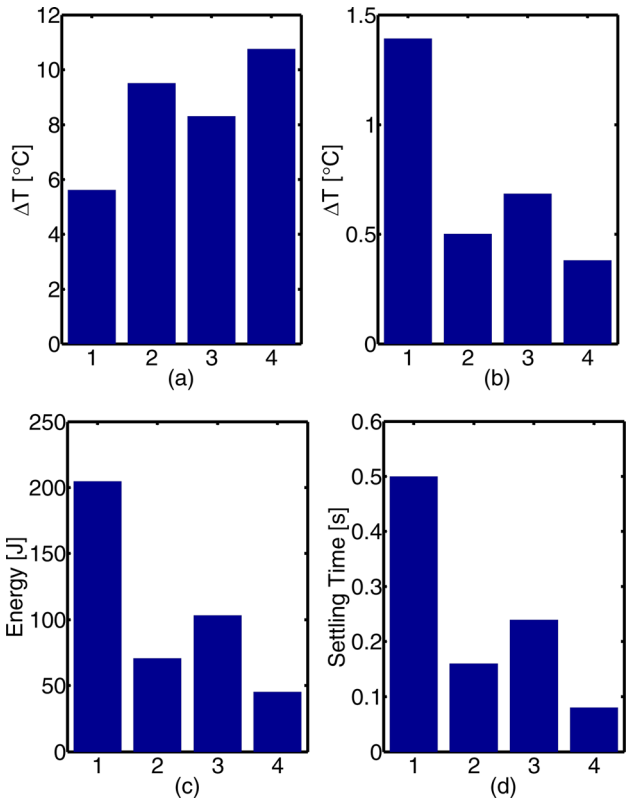


Fig. 10 Comparison of the four pulses: (1) Constant, (2) Linear, (3) Square Root and (4) Parabolic using four parameters important to select a pulse: (*a*) Difference between maximum temperature and threshold temperature ($\sim$102 °C), (*b*) Temperature overshoot after pulse is turned off, (*c*) Total energy expended during pulsed operation and (*d*) Settling time for temperature within 0.5 °C of steady-state

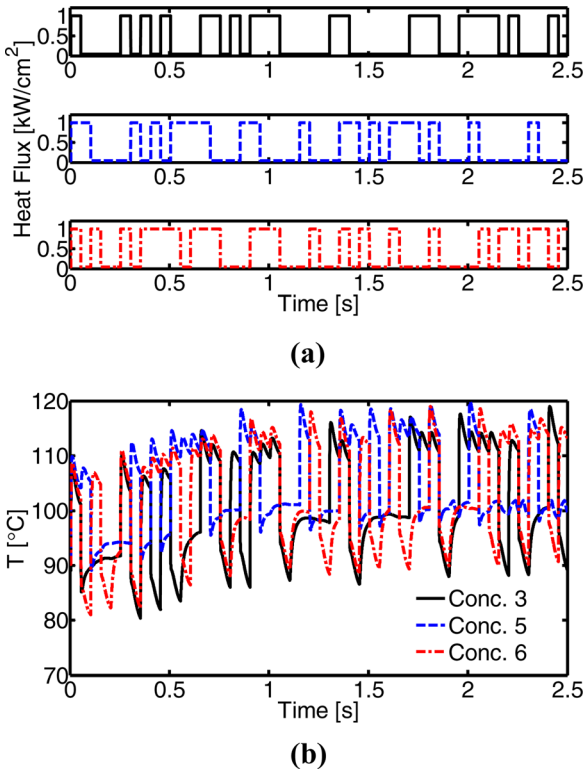


Fig. 11 (*a*) Random cycling of hot spots 3, 5 and 6, respectively; (*b*) Transient temperature at hot spots when TECs turned on with square root pulse at hot spot temperature >102 °C during random cycling of hot spots

5.2 Temperature Control of Random Hot Spot. Location of hot spots on chip can vary with time. Multiple TECs integrated inside an electronic package should be able to manage high heat fluxes originating from these hot spots according to their spatio-temporal variation. The following study implements a simple maximum temperature control, which turns on the corresponding TECs as soon as the hot spot's temperature reaches a preset threshold temperature. To test this control of hot spot temperature by TECs, a simulation is performed with three hot spots: hot spots at location 3, 5 and 6 in Fig. 1(*b*), which turn on randomly with 0.05 second period. Once the hot spot reaches 102 °C, the TECs corresponding to these hot spots are turned on with a square root pulse of amplitude 8 A and duration of 0.05 s; after 0.05 s TECs are switched to inactive mode ($\sim$no current through TECs). Figure 11(*a*) shows the random cycling of the hot spots, and Fig. 11(*b*) shows the temperature of three hot spots. The square root pulse is capable of cooling the chip below the temperature with zero current in TEC for the first 0.75 s, but transient cooling with the TEC is no longer effective after this point. The Joule heating in the TECs continues to heat the entire chip and thus over long periods of time, the temperature continues to rise. By the end of the

2.5 s simulation, temperatures on chip appear to have approached a steady periodic temperature but are approximately 3–4 °C higher than temperatures with no TEC cooling. Therefore, transient cooling with high amplitude current pulses is effective for infrequent short period hot spots, but for frequent hot spots, current values closer to steady-state (∼3A instead of 8A) should be utilized to provide cooling without the degradation over time. The present analysis of temperature control of random hot spots is a sample case study to observe the behavior of an electronic package with random hot spots under pulsed TEC operation. The intensity of heat flux and transient temperature rise at hot spot location in addition to the thermal behavior of the surrounding need to be appropriately considered for an energy efficient control of hot spots by TECs. Further investigation need to be performed to determine better dynamic control techniques to manage multiple hot spots.

6 Conclusion

We have developed a computational model to analyze the cooling of hot spots on a chip using nine Peltier coolers attached at the bottom side of the heat spreader. We have investigated the effect of both steady state and transient modes of operation of the TECs for hot spot temperature reduction. Steady-state results show that conductive coupling between active TECs can be very strong. Joule heating in one TEC device can negatively affect operation of adjacent TECs, but the increase in thermal spreading can also help to reduce peak temperatures on chip. Transient results for multiple TECs show a small decrease in response time and a small increase in maximum achievable cooling due to the conductive coupling of multiple TECs. Further transient analysis shows that varying shapes of pulses passed through the TEC can significantly affect the cooling achieved and can be optimized for different parameters such as total energy consumed, maximum temperature, maximum overshoot and settling time. The square root pulse proved to be the most effective with degree of cooling (∼10 °C) similar to the constant amplitude or step pulse but half of the energy consumption compared to the step pulse. Initial tests were performed for transient cooling of random hot spots by multiple TECs with high amplitude current pulses. The results were promising for short term infrequent hot spots, but transient cooling eventually leads to high temperatures at hot spots if used continuously over a long period of time. For efficient utilization of TECs, further optimization of pulses need to be performed and dynamic control algorithms need to be developed.

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