# Hotspot Cooling in Stacked Chips Using Thermoelectric Coolers

Matthew Redmond, Kavin Manickaraj, Owen Sullivan, Saibal Mukhopadhyay, *Senior Member, IEEE*, and Satish Kumar

***Abstract*— 3-D technologies with stacked chips have the potential to provide new chip architecture, and improved device density, performance, efficiency, and bandwidth. The increased power density in 3-D technologies can become a daunting challenge for heat removal. Furthermore, power density can be highly nonuniform, leading to time- and space-varying hotspots, which can severely affect performance and reliability of integrated circuits. It is important to mitigate on-chip thermal gradients while considering the associated cooling costs. One efficient method of hotspot thermal management is to use superlattice thermoelectric coolers (TECs), which can provide on demand and localized cooling. In this paper, a detailed 3-D thermal model of a stacked electronic package with two dies and four ultrathin integrated TECs is developed to investigate the efficacy of TECs in hotspot cooling for 3-D technology. A strong vertical coupling has been observed between TECs located in top and bottom dies. Bottom TECs can significantly heat the top hotspots in both steady-state and transient operation. TECs need to be carefully placed inside the package to avoid such undesired heating. Thermal contact resistances between dies, inside the TEC module, and between TEC and heat spreader are shown to have a crucial effect on the TEC performance. We observe up to 5.6 °C of active hotspot cooling in steady state and 7.4 °C of active hotspot cooling using a square root current pulse.**

***Index Terms*— Contact resistance, electronics cooling, integrated circuit packaging, thermoelectric devices, through-silicon vias.**

## I. Introduction

As microelectronic device size continues to be reduced, a physical limit will inevitably be reached. Current research efforts focus on new ways to improve the performance of microelectronic devices. One such avenue, 3-D stacked chips, involves stacking several active dies interconnected through silicon vias (TSVs). This novel architecture may reduce microelectronic form factor, improve performance by reducing interconnect delay, and provide a more energy-efficient chip design [1]–[3]. However, these electrical and packaging benefits may be offset by the thermal concerns.

Increased power density can become a daunting challenge for heat removal in the 3-D technology. Though it has been suggested that TSVs can be used for circuit-level thermal management, it is expected that widespread adoption of the 3-D technology will bring severe thermal management challenges at the package level [1], [4]. A severe thermal challenge in chips is the formation of hotspots, which occur on varying time and spatial scales and are caused by the high packing densities typical in modern chips [5], [6]. These hotspots, if not adequately cooled, result in temperature gradients, which hurt chip performance and reliability [7]. Modern chips generate average heat fluxes of around 100 W/cm$^2$, but localized heat fluxes can be up to five times higher [8]–[10].

Multiple efforts are underway to develop new methods of efficient cooling in 3-D electronics. These efforts include the use of microchannels, high-conductivity thermal interface materials, and solid-state thermoelectric coolers (TECs) [5], [11]–[15]. Hybrid cooling systems including fluidic microchannels and TECs have also been investigated for hotspot cooling [16], [17]. Though microchannels are suitable for high-performance applications where extreme heat fluxes are present, manufacturing can become very challenging. Since hotspots occur on varying temporal and spatial scales, cooling methods should be scalable on demand and actively controlled to cool hotspots as necessary. This is important to improve efficiency and reduce cooling costs [18].

TECs are particularly suitable for on demand and actively controlled cooling at hotspots. TECs are solid-state devices in which the operation is based on the Peltier effect. These devices output a temperature difference when a voltage is applied and can conversely output a voltage when a temperature difference is applied. In either function, they have the potential to play a role in sustainable technology innovations [19], [20]. They have no moving parts and are therefore silent, reliable, and scalable [10], [21]. These qualities make them a good solution for distributed and on-demand cooling.

The figure of merit, $ZT = S^2\sigma T/k$, is used to describe the efficiency of a thermoelectric material [21]. Here, $S$ is the Seebeck coefficient, $\sigma$ is the electrical conductivity, $T$ is the average temperature of the device, and $k$ is the thermal conductivity. Although thermoelectric devices are generally inefficient, materials with a figure of merit greater than 2 have been created through the use of nanostructures, and reducing the thickness of TECs can further increase their performance [5], [22]. Ultrathin ($\sim$100 $\mu$m) TECs with 8-$\mu$m-

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thick $Bi_2Te_3$ superlattices have been successfully integrated at the back of a heat spreader and shown to provide up to 15 °C cooling at hotspots [5]. However, thermal and electrical contact resistances inside a TEC and at the TEC-package interface limit their performance and effectiveness [5].

In transient operation, TECs are able to produce additional cooling through current pulses over that which can be achieved in steady-state operation [23]–[25]. The cool side of TEC experiences the Peltier cooling immediately when an electrical current pulse is applied, whereas the Joule heating occurring within TEC takes a longer time to propagate to the surface. This causes a temporary supercooling effect, which may be followed by an overshoot in temperature once the cooling load is removed. The shape of the current pulse can be optimized to increase the cooling effect and reduce the temperature overshoot [26].

Various studies have been performed in the areas of 3-D integrated circuits, electronics packaging, hotspot thermal management, and TECs. Detailed computational models of TECs integrated into a 2-D electronic package have shown that the transient operation of TECs can reduce the hotspot temperature by 6 °C–7 °C, in addition to cooling achieved in the steady-state operation of TEC [27]. It has also been shown that a square root pulse provides more effective transient cooling than a constant pulse for 2-D chips [26]. The previous studies have reported that a large increase of thermal contact resistances greatly degrades or negates the cooling provided by TECs [27]–[29]. Other studies have envisioned the use of thermoelectric heat spreading in stacked chips [30] or a TEC combined with a silicon interposer [31] to cool hotspots, but a detailed investigation of the application of TECs in a 3-D stacked-chip package for hotspot thermal management has not yet been performed.

In this paper, a detailed 3-D thermal model of two stacked dies with four ultrathin (∼100 $\mu$m) TECs has been developed to investigate the performance of TECs in providing steady-state or on demand transient cooling at hotspots in stacked-chip architecture. First, the steady-state performance of TECs in both active and passive state with varying current magnitudes is explored. The coupling between TECs and their effectiveness in providing cooling at different hotspot locations on dies during their simultaneous operation is studied. An instance of unequal power on two dies is investigated to consider the case of different die functionalities (e.g., logic and memory). Next, variation of the thermal contact resistances between dies, inside the TEC module, and between TEC and the heat spreader is examined. Finally, the transient performance of TECs under varying current amplitudes and pulse shapes is explored.

## II. Computational Methodology

In order to analyze the effect of TECs on the hotspot temperature reduction in a stacked die, a computational model of four TECs integrated into a stacked-chip electronic package was developed. A schematic of the electronic package, TECs, and hotspot locations are shown in Fig. 1. A bottom chip is mounted on a substrate and a top chip is attached to the bottom

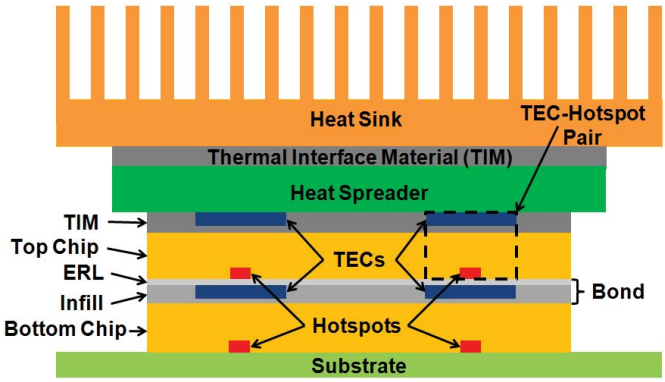


Fig. 1. Schematic of the electronic package. Heat sink, heat spreader, chip, thermal interface material (TIM), effective resistance layer (ERL), infill, hotspot locations, TECs, and substrate are shown.

chip. The bonding method of the chips is left unspecified because bonding in the 3-D stacked chips has been proposed using many different methods [2], [3]. For generality, the bond is represented by a thin effective resistance layer (ERL) and an infill layer. The thermal conductivity of the ERL can be varied, so the effect of different bonding techniques on the thermal performance of an electronic package with integrated TECs can be investigated. The infill is presumed to be a compliant polymer, similar to modern underfill or TIM, which enhances both mechanical stability and thermal performance of the package. Four TECs, each 100-$\mu$m thick and composed of $7\times7$ p-n couples, are paired with two hotspots on the bottom and two hotspots on the top chip. The top TECs are attached to the heat spreader while the bottom TECs are attached to the ERL. The computational domain includes the heat spreader, chips, TIM, ERL, infill, hotspots, and TECs.

The substrate is considered as an adiabatic interface and the heat sink is modeled using a 2050 W/m$^2$-K convective boundary condition with an ambient temperature of 300 K for computational simplicity. The four hotspots are represented by four high heat flux sources of magnitude 1000 W/cm$^2$ and area $400\times400$ $\mu$m located at the bottom of their respective chips. A uniform heat flux of 14.5 W/cm$^2$ is considered for the rest of the chip area. The total power dissipation is 23.9 W per chip, or 47.8 W for the electronic package unless mentioned differently. The effective heat flux of the top and bottom chips are described by (1)

$$q'' = \begin{cases} 1000\ \frac{W}{\text{cm}^2}, & \text{at the hot spots} \\ 14.5\ \frac{W}{\text{cm}^2}, & \text{elsewhere.} \end{cases} \quad (1)$$

The effective thermoelectric properties of the $Bi_2Te_3$-based thin-film superlattice material are considered for modeling thermoelectric (TE) material in the 100-$\mu$m-thick TEC modules. In each TEC module, an 8-$\mu$m-thick $Bi_2Te_3$-based TE material is sandwiched between two copper layers. The effective thermal conductivity of this TE material was experimentally measured to be 1.2 W/m-K in [5]. The thermal conductivity of the TIM was also determined experimentally to be 1.75 W/m-K in [5]. Electrical and thermal resistances at the interface of the TE-copper layers ($10^{-11}$ $\Omega$m$^2$; $1\times10^{-6}$ m$^2$-K/W) inside the TEC module and at the interface

TABLE I
DIMENSIONS AND MATERIAL PROPERTIES OF THE ELECTRONIC PACKAGE COMPONENTS

| Component | Thermal Conductivity (W/m-K) | Dimensions (mm × mm × mm) |
|---|---|---|
| ERL | 5 | 13 × 11 × 0.025 |
| Chip | 140 | 13 × 11 × 0.5 |
| Heat spreader | 400 | 30 × 30 × 1 |
| Infill | 1.75 | 13 × 11 × 0.125 |
| TEC, copper | 400 | 3 × 3 × 0.046 |
| TEC, superlattice | 1.2 [5] | 3 × 3 × 0.008 |
| TIM | 1.75 [5] | 13 × 11 × 0.125 |

of the TEC-spreader ($8 \times 10^{-6}$ m$^2$-K/W) are also taken from [5]. Selected dimensions and material properties for the model are listed in Table I.

Peltier cooling is a surface effect, which is incorporated by adding heat ($\sim$SIT$_h$) at the hot side and subtracting heat ($\sim$SIT$_c$) from the cold side of the TE material. Here, $T_h$ and $T_c$ are the hot and cold-junction temperatures, respectively, and $I$ is the applied current. $S$ is taken as 300 $\mu$V/K based on the experimental measurement in [5]. The Joule heating inside the TEC module and at the interfaces ($\sim$electrical contact resistance at TE-copper interface) is modeled by adding source terms of magnitude $I^2R$ at the corresponding volumes and interfaces.

The details of the TEC model can be found in our previous work on TECs integrated with a 2-D electronic package [27].

*1) Governing Equations:* Fourier's equation for conduction heat transfer in three dimensions is given as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{\dot{q}}{k} = \frac{\partial T}{\alpha \partial t} \tag{2}$$

where

$$\dot{q} = \begin{cases} \frac{I^2}{\sigma A^2}, & \text{inside TEC} \\ 0, & \text{elsewhere.} \end{cases} \tag{3}$$

In the equations, $T$ is temperature, $\dot{q}$ is volumetric heat generation, $k$ is thermal conductivity, $\alpha$ is thermal diffusivity, $I$ is current, $\sigma$ is electrical conductivity, and $A$ is the area of TEC.

*2) Boundary Conditions:* The effects of the Peltier cooling and the Joule heating at the electrical contact resistances are considered at the cold end of the TE material

$$-kA\frac{\partial T}{\partial y}\Big|_{y=y_c^+} = \left[-kA\frac{\partial T}{\partial y} - SIT\right]_{y=y_c^-} + I^2 R_{\text{elec}} \tag{4}$$

and at the hot end of the TE material

$$-kA\frac{\partial T}{\partial y}\Big|_{y=y_h^+} = \left[-kA\frac{\partial T}{\partial y} - SIT\right]_{y=y_h^-} + I^2 R_{\text{elec}}. \tag{5}$$

In these equations, $S$ is the Seebeck coefficient and $R_{\text{elec}}$ is the electrical contact resistance at the appropriate interface. In addition, $y_c^+$, $y_c^-$, $y_h^+$, and $y_h^-$ are locations just above and below the hot and cold junctions.

Simulations are performed using the finite volume-based commercial solver FLUENT. User-defined functions are developed to evaluate the temperature at the hot and cold junctions, which is further used to estimate the temperature-dependent Peltier cooling and heating terms ($\sim$SIT) in (4) and (5). For steady state, the temperature is solved iteratively until convergence in a self-consistent fashion to ensure that the Peltier cooling terms use the right values of the hot and cold-junction temperatures. For the transient simulations, the explicit temperature of the hot and cold junction was used for the duration of a time step. The present computational model contains 158 000 cells. Grid independence tests performed using 2.9 million cells yield very small changes in temperature distribution and verify that 158 000 cells are sufficient for the numerical simulations. Typical steady-state temperature contour plots in a horizontal plane through the bottom chip and in a vertical cross section of the electronic package are shown in Figs. 2 and 3.

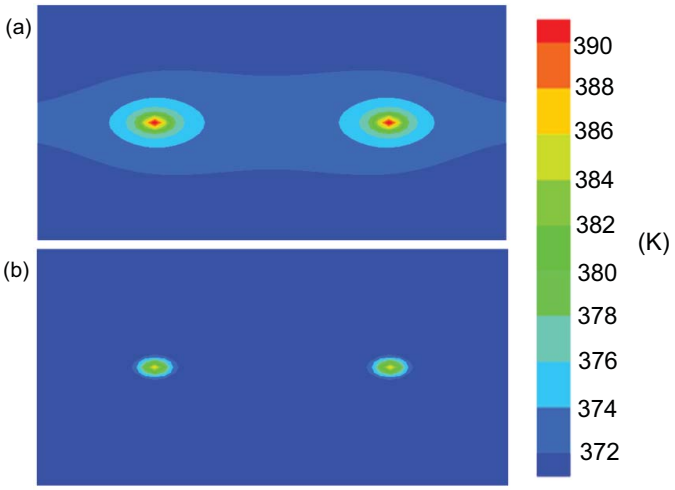


Fig. 2. Temperature contour plot in a horizontal plane through bottom chip showing hotspot temperatures. (a) Temperature contour with 0 A through all four TECs. (b) Temperature contour with 1.75 A through all four TECs.

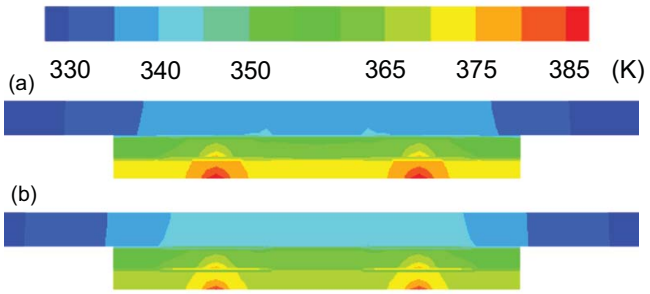


Fig. 3. Temperature contour in a vertical cross section of electronic package. (a) Temperature contour with 0 A current through all four TECs. (b) Temperature contour with 1.75 A current through all four TECs.

## III. STEADY-STATE PELTIER COOLING AT HOTSPOT

### A. Active and Passive Cooling

A benchmark analysis was performed to see the variation in maximum temperatures on the chip without TECs, with TECs, and with 100-$\mu$m-thick copper blocks in place of TECs. A significant amount of passive cooling, or cooling without an applied current, was observed in [5] because of the high

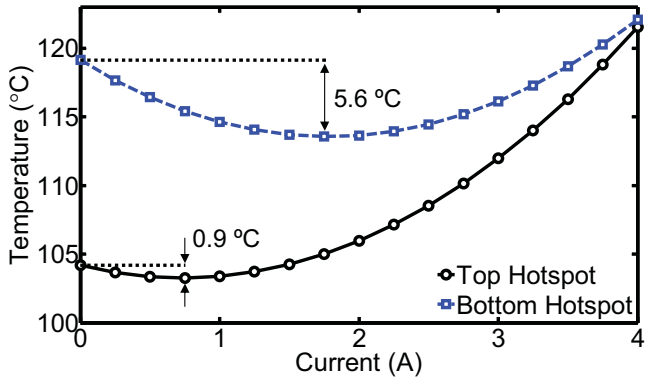


Fig. 4. Hotspot temperature variation with applied current in TECs. Current through all four TECs is the same.

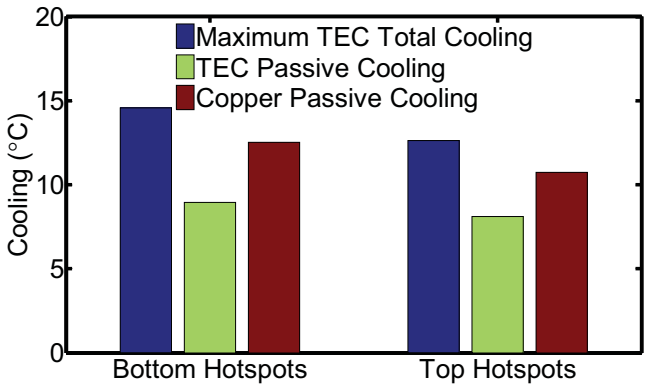


Fig. 5. Comparison of maximum TEC total cooling (active + passive), TEC passive cooling, and passive cooling by 100-$\mu$m-thick copper pieces.

thermal conductivity of copper making up a large portion of the device. In our model, integrating TECs causes passive cooling of 8.9 °C at the bottom hotspots and a passive cooling of 8.1 °C at the top hotspots compared with the chip without TECs. However, the passive cooling by 100-$\mu$m-thick copper blocks is larger (12.5 °C at the bottom hotspots and 10.7 °C at the top hotspots) than passive cooling by TECs as the effective conductivity of the TEC module is lower than copper. The value of integrating a TEC in a package cannot come from its passive cooling, but must come from its ability to provide active, on-demand cooling.

Next, a steady-state analysis was performed by applying the same current to all four TECs in the range of 0–4 A. Fig. 4 shows that the maximum active cooling at the top hotspot is only 0.9 °C corresponding to 0.75 A current through all four TECs. Active cooling of 5.6 °C is observed at the bottom hotspots when 1.75 A current is applied through TECs. As the applied current magnitude increases, the Peltier cooling effect is eventually overcome by the detrimental Joule heating effect occurring within TECs and the contacts. It is important to notice that the top-chip experiences small amounts of active cooling with all four TECs active at an equal constant current. Later sections of this paper show that this is due to heating of the top hotspots by the bottom TECs.

To explore the best possible cooling at top and bottom hotspots by TECs, we next apply current with different magnitudes in top and bottom TECs in the range of 0–3 A rather than keeping them at the same value. The maximum total cooling at the top hotspots was observed to be 12.6 °C (~4.5 °C active). This cooling was observed for a top current, $I_t$, equal to 2.5 A and a bottom current, $I_b$, equal to 0 A. The maximum total cooling at the bottom hotspots was observed to be 14.6 °C (~5.6 °C active). This cooling was observed for a top current, $I_t$, equal to 2.0 A and a bottom current, $I_b$, equal to 1.75 A. These results are similar in magnitude to those observed in [5], [27], and [28]. Fig. 5 compares the maximum total cooling (active + passive) obtained by TECs with the passive cooling obtained by TECs or copper blocks. It is clear that the active cooling achieved using TECs is higher than the passive cooling using copper blocks. Furthermore, TECs can be fabricated directly on chip using microelectromechanical systems processes, or the thickness of a TEC can be further decreased. This would diminish the passive cooling effects of both TECs and copper blocks, whereas the active cooling effects of TECs would remain approximately the same.

It was also observed that small changes in the applied currents yielding the maximum active cooling did not significantly change the observed cooling. It is desirable to use applied currents as small as possible in an effort to reduce energy consumption in TECs. Using 20% less current in the top TECs (2.0 versus 2.5 A) and no current in bottom TECs leads to only a 5% decrease in the active cooling of the top hotspots (4.3 °C versus 4.5 °C). Similarly, reductions of top and bottom TEC current by 0.5 A (1.5 versus 2.0 A for top current; 1.25 versus 1.75 A for bottom current) results in only a 6% decrease in active cooling for the bottom hotspot (5.3 °C versus 5.6 °C). This suggests that lower currents might be used to obtain similar cooling performance with significant energy savings as the Joule heating is proportional to current squared.

The goal of these studies was not to optimize the current through TECs, but to explore the effects of different current magnitudes. These studies suggest that, in steady state, current magnitudes of 1.75 A provide a balance of cooling and energy consumption. For this reason, 1.75 A current magnitudes are extensively used in the steady-state portion of this paper.

### *B. Effect of TEC Location on Hotspots*

A study was performed to determine the contribution to hotspot cooling by a TEC at various locations relative to the hotspot. Beginning with zero applied current to all TECs, a 1.75 A current was applied to a single TEC under consideration. Temperature drops or rises were recorded for all hotspots along with the locations of the hotspots and activated TEC. This was repeated for all four TECs. This same procedure was performed for starting configurations where 1, 2, or 3 of TECs already had an applied current of 1.75 A, and a 1.75 A current was applied to a nonactive TEC. It was observed that the cooling at a single hotspot was dependent only on the activated TECs location and independent of the starting configuration or magnitude of applied current to other TECs. This can be explained using the superposition principle which applies to linear systems. TECs caused negligible horizontal (0.05 °C) and diagonal (0.3 °C) cooling (see Fig. 1 for TEC locations).

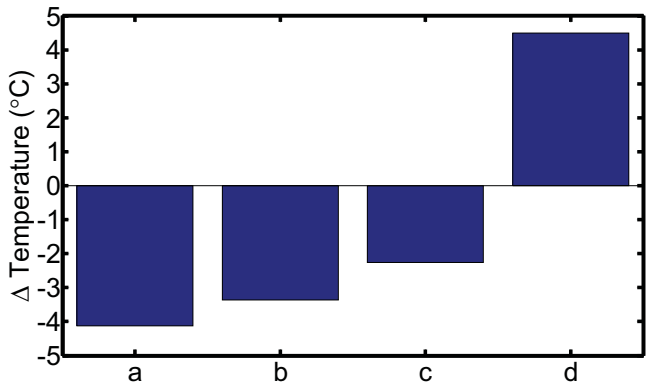


Fig. 6. Change in peak hotspot temperature as a result of activating additional TECs with 1.75 A current. (a) Cooling on top hotspot caused by activating top TEC. (b) Cooling on bottom hotspot caused by activating bottom TEC. (c) Cooling of bottom hotspot caused by activating top TEC located at same horizontal location. (d) Heating of top hotspot caused by activating bottom TEC located at same horizontal location (see Fig. 1 for TEC locations).

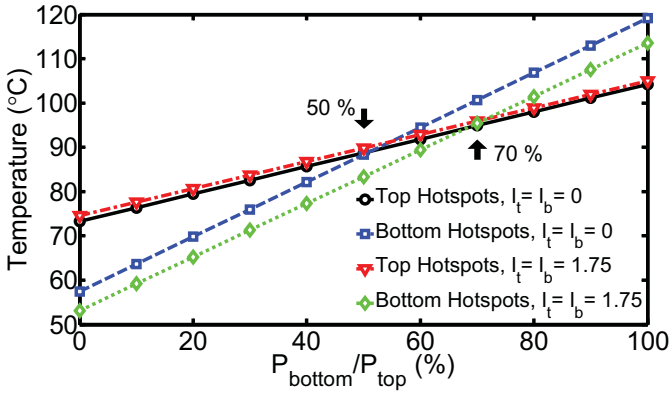


Fig. 7. Top-chip power is held constant and the power of the bottom chip is varied as a percentage of the top-chip power. Same current is applied through all four TECs.

However, significant vertical coupling between TECs and hotspots was observed as shown in Fig. 6.

As expected, applying a current to a TEC causes a cooling effect to the hotspots below that TEC and a heating effect above that TEC. For example, if a 1.75 A current is applied to the top TEC, it cools both the top and bottom hotspots Fig. 6(a) and (c). However, if a 1.75 A current is applied to the bottom TEC, it cools the bottom hotspot Fig. 6(b), but heats the top hotspot Fig. 6(d). It is important to ensure that the heating of the top hotspot is not too severe. In the case of the modeled electronic package, the bottom hotspot temperatures are much higher than the top hotspot temperatures, so cooling the bottom hotspots at the cost of heating the top hotspots is acceptable.

### C. Unequal Power on Chips

In a stacked-chip architecture, it is possible to have different functionalities (e.g., logic, memory, etc.) equivalently located on different dies, which will lead to equal power dissipation on different stacked dies or chips. Alternatively, a die can be dedicated to memory and another die to logic leading to unequal power dissipation on different dies. From a thermal perspective, it is advantageous to place the higher power chip or die near the heat sink to reduce peak temperatures of the electronic package. We modeled the electronic package with the top chip having higher power. The bottom-chip power was varied as a percentage of the top-chip power while the top-chip power was held constant. The current through all four TECs was set to either 0 or 1.75 A, and the hotspot temperatures were investigated. The results of this analysis are shown in Fig. 7. If no current is applied to TECs, bottom- and top-chip peak temperatures are equal when the bottom chip dissipates about 50% power of the top chip (arrow in Fig. 7). If the applied current through all four TECs is 1.75 A, bottom- and top-chip peak temperatures are equal when the bottom-chip power is about 70% of the top-chip power (arrow in Fig. 7). The TECs in the stacked-chip architecture can provide cooling necessary to increase bottom-chip power.

## IV. Effect of ERL and Thermal Contact Resistances

### A. ERL

Different die-bonding techniques in the 3-D stacked chips have been investigated in previous studies [2], [3]. A thin (25 $\mu$m) ERL was considered between the top and bottom die (see Fig. 1) to study the how the thermal resistances of bonding materials and interfaces may affect the thermal performance of TECs. The thermal conductivity of the ERL was varied between 1 and 10 W/m-K and the current through all four TECs was set to 0 or 1.75 A. The ERL conductivity had a negligible effect on the top hotspot temperatures ($< 0.3$ °C). Fig. 8 shows the results of this analysis for the bottom hotspot temperature. Changing the ERL conductivity from 1 to 10 W/m-K results in a 4.73 °C reduction of the bottom hotspot temperature when all four TECs are inactive (0 A applied current) and a 6.72 °C reduction of the bottom hotspot temperature when all four TECs are active with 1.75 A applied current. A majority of this cooling is observed as the ERL conductivity is changed from 1 to 5 W/m-K.

### B. Superlattice-Copper Contact Resistance

The superlattice-copper contact resistance inside a TEC module is dependent on the fabrication process. This contact resistance, $R_c$, is measured to be in the order of $1 \times 10^{-6}$ m$^2$K/W in [5]. New technologies can reduce the contact resistance whereas fabrication defects can increase the contact resistance. To quantify these effects, the superlattice-copper contact resistance was varied by one order of magnitude higher and lower from the value reported in [5]. The current through all four TECs was set to 0 or 1.75 A. The results of this analysis are shown in Fig. 9. The superlattice-copper contact resistance, $R_c$, has a more dramatic effect on temperature at higher applied currents (1.75 versus 0 A). An increase in the contact resistance by one order of magnitude to $1 \times 10^{-5}$ m$^2$K/W can result in 8 °C increase in the bottom hotspot temperature, but decreasing contact resistance by an order of magnitude to $1 \times 10^{-7}$ m$^2$K/W results in only 1 °C–2°C decrease in the hotspot temperature.

The coefficient of performance (COP) of the bottom and top TECs was also determined for two superlattice-copper thermal

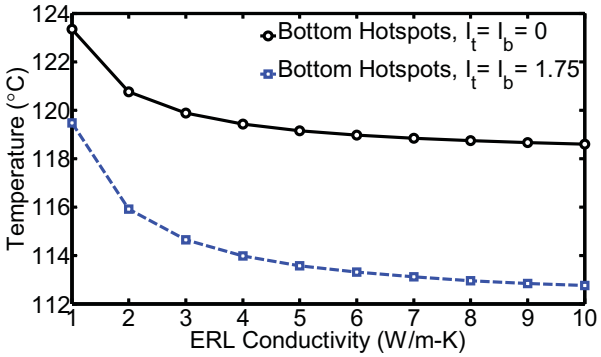


Fig. 8. Bottom hotspot temperature with varying ERL conductivity. The applied current to all four TECs is the same.

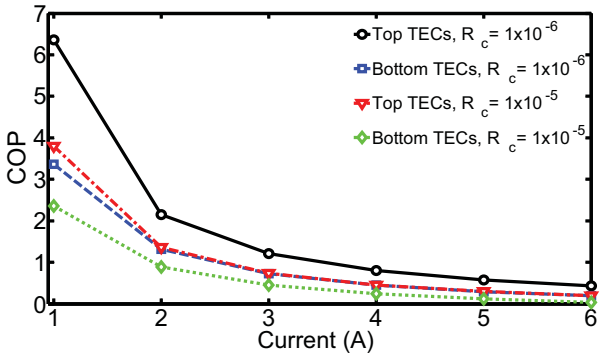


Fig. 10. Bottom and top TEC COPs with varying current. The superlattice-copper contact resistance is either $1 \times 10^{-6}$ m$^2$K/W or $1 \times 10^{-5}$ m$^2$K/W.

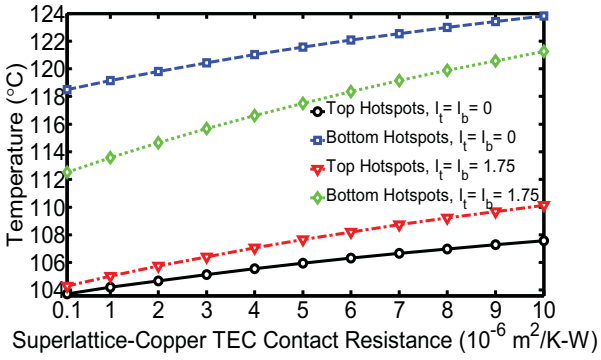


Fig. 9. Bottom and top hotspot temperatures with varying superlattice-copper contact resistance. The current through all four TECs is set at 1.75 or 0 A.

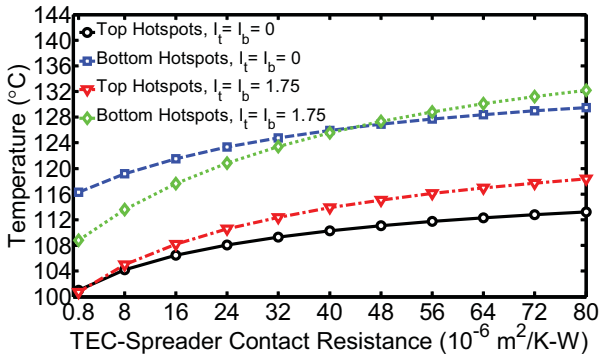


Fig. 11. Bottom and top hotspot temperatures with varying TEC-spreader contact resistance. The current through all four TECs is set at 1.75 or 0 A.

contact resistances at various applied currents. The COP for a TEC is defined as the difference in the amount of heat flux at the cold end of TEC with and without an applied current divided by the power consumed by that TEC. The power consumed by a TEC consists of the Joule heating (bulk and contacts) and the power required to create the Peltier cooling effect. The Joule heating power is a function of only electrical resistances and the current, but the power required to create the Peltier cooling effect is dependent on both electrical and thermal inputs, and is described by (6)

$$P_{\text{peltier}} = NSI(T_h - T_c) \tag{6}$$

where $N$ is the number of thermoelectric elements, $S$ is the Seebeck coefficient, $I$ is the applied current, and $T_h$ and $T_c$ are the hot and cold-junction temperatures, respectively. This calculation is explained in more detail in [32]. The electrical contact resistance of the superlattice-copper interface was held constant. An increase in the superlattice-copper thermal contact resistance from $1 \times 10^{-6}$ m$^2$K/W to $1 \times 10^{-5}$ m$^2$K/W resulted in decreased COP (Fig. 10). Furthermore, the top TECs had higher COP than the bottom TECs. This is likely because the top TECs are closer to the heat spreader than the bottom TECs and are better able to reject heat. The thermal resistance can have a crucial effect on COP.

### C. TEC-Spreader Contact Resistance

The TEC-spreader contact resistance can have a significant effect on the operation of TECs inside an electronic package. To quantify these effects, the TEC-spreader contact resistance was varied by one order of magnitude higher and lower from its value of $8 \times 10^{-6}$ m$^2$K/W observed in [5]. The current through all four TECs was set to 0 or 1.75 A, respectively. The results of this analysis are shown in Fig. 11. Similar to the superlattice-copper contact resistance, the TEC-spreader contact resistance has a more dramatic effect on temperature at higher applied currents (1.75 versus 0 A). Increasing the TEC-spreader contact resistance to $8 \times 10^{-5}$ m$^2$K/W results in up to an 18.6 °C increase in the bottom hotspot temperature. In addition, reducing the TEC-spreader contact resistance to $8 \times 10^{-7}$ m$^2$K/W, can result in a 4.8 °C reduction in the bottom hotspot temperature. The hotspot temperatures are observed to be more sensitive to the TEC-spreader contact resistance when compared with the superlattice-copper contact resistance, because the contact resistance at the TEC-spreader interface is higher. The contact resistance at the TEC-spreader interface can become so large, that it is better to keep TECs off. Significant attention is deserved to find ways to reduce this contact resistance to effectively utilize TECs in stacked chips.

## V. Transient Pulse Analysis

### A. Transient Cooling With Step Input Currents

A transient current pulse through a TEC has been shown to provide cooling to a greater extent than the steady-state cooling by a TEC [24], [27], [28]. The steady-state temperature distribution of the electronic package with zero current

through TECs was used as an initial state for this analysis. A time step of 0.002 s was used for the initial transient simulations. It is observed that the application of the same current magnitude to all four TECs leads to cooling in the bottom hotspots, but heating at the top hotspots. This top hotspot heating is prohibitive (>2 °C) when large currents are applied to bottom TECs, even though these large current pulses can lead to a high degree of cooling at the bottom hotspots. Larger applied currents produce a faster response than smaller currents, but are accompanied by the Joule heating resulting in a large temperature overshoot after the minima in temperature is achieved. The temperature minimum at the bottom hotspots occurs between 0.05 and 0.1 s depending on the magnitude of the applied current. A fast response time is desirable for transient cooling of hotspots because hotspots can appear and disappear in the order of milliseconds.

In an effort to find TEC current amplitudes appropriate for use in this model, two measures were defined to quantify the suitability of the current magnitude used in cooling. The amount of cooling at bottom hotspots that occurs 0.05 s after the application of a step input current was used to quantify the degree of cooling that occurs quickly enough to be useful in transient heat removal from an electronic package. The maximum amount of heating at the top hotspots within 0.05 s after applying a step current in TECs quantified the negative effects that TECs may have on the top hotspots. The objective here was to find the maximum cooling of the bottom hotspot while preventing top hotspot heating of more than 2 °C. With these objectives, the transient performance of TECs in the electronic package was modeled using current amplitudes between 2 and 4 A on the bottom TECs while the current amplitudes of the top TEC were varied between 2 and 10 A. The two measures previously defined were used to quantify the results. The maximum heating that occurs at the top hotspots within the first 0.05 s is shown in Fig. 12(a). The cooling at the bottom hotspots at 0.05 s is shown in Fig. 12(b). Based on the criterion described above, a bottom TEC current of 3 A and a top TEC current of 8 A provides the maximum bottom hotspot cooling but limits top hotspot heating under 2 °C. These current amplitudes are used in the pulse shape analysis in the next section.

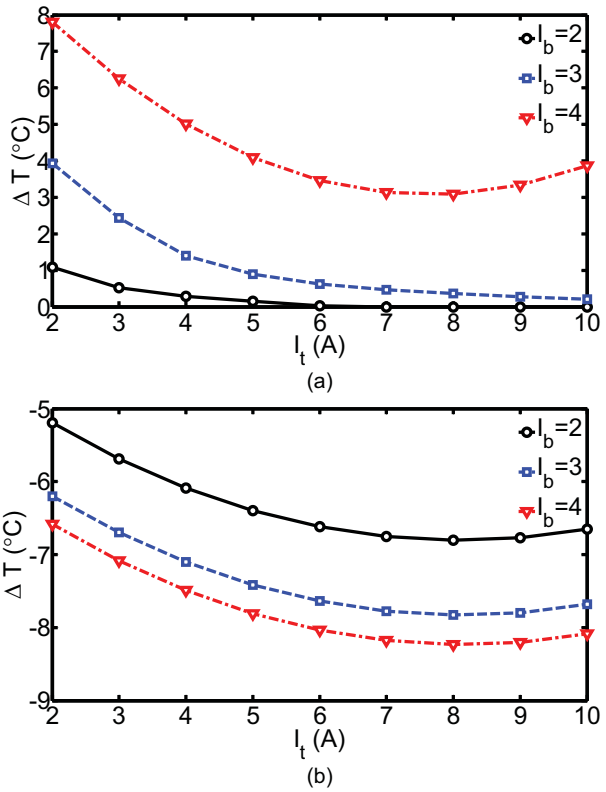


Fig. 12. Bottom TEC current ($I_b$) is varied between 2 and 4 A, while the top TEC current ($I_t$) is varied between 2 and 10 A. (a) Maximum heating on the top hotspots within the first 0.05 s. (b) Cooling on the bottom hotspots at 0.05 s.

### *B. Pulse Shape Investigation*

Using a top TEC current amplitude of 8 A and a bottom TEC current amplitude of 3 A, various current pulse shapes of duration 0.05 s were investigated for use in bottom-chip cooling. In this analysis, a time step of $2 \times 10^{-4}$ s was used to calculate the hotspot temperature profiles. This time step is one order of magnitude smaller than that used in the previous section. The pulse shapes under consideration were: constant ($t^0$), linear ($t^1$), quadratic ($t^2$), and square root ($t^{1/2}$). These pulse shapes have been discussed in detail in [28].

The results of this investigation are shown in Fig. 13. The constant current pulse provided the maximum cooling at the bottom hotspot with a 7.9 °C temperature drop at 0.05 s. The square root pulse provided a slightly smaller (~7.4 °C) temperature drop Fig. 13(b). None of the current pulses produced a significant amount of heating on the top hotspot, although it should be noted that the constant current pulse is the only pulse that causes a temperature spike (<1 °C) at the top hotspot just after the application of current pulse Fig. 13(a). This temperature spike is similar to that observed by the constant current step inputs applied in the previous section.

Interesting behavior is observed for the top hotspot temperatures for all pulse shapes. During the first 0.05 s period, the top hotspot temperature first decreases because of the Peltier cooling at the surface, and then begins to rise because of the Joule heating within TECs. This is due to the shorter response time of the Peltier cooling surface effect compared with the Joule heating within TECs. However, when TECs become inactive at 0.05 s, a temperature drop ensues as the temperature at the bottom TEC hot side instantly decreases as the Peltier effect is removed. This temporary temperature drop quickly disappears, and temperature overshoot above the initial temperature appears, as expected. The overshoot is greatest for the constant current pulse Fig. 13(a).

The COP of TECs is typically low, especially at large current amplitudes, and energy consumption throughout the current pulse needs to be carefully considered. A constant current pulse produces 50% more Joule heating than a square root pulse of the same amplitude [28], but the maximum degree of cooling is nearly the same for these two pulses. This energy-saving quality of square root pulses in particular, combined with their similar performance to constant current

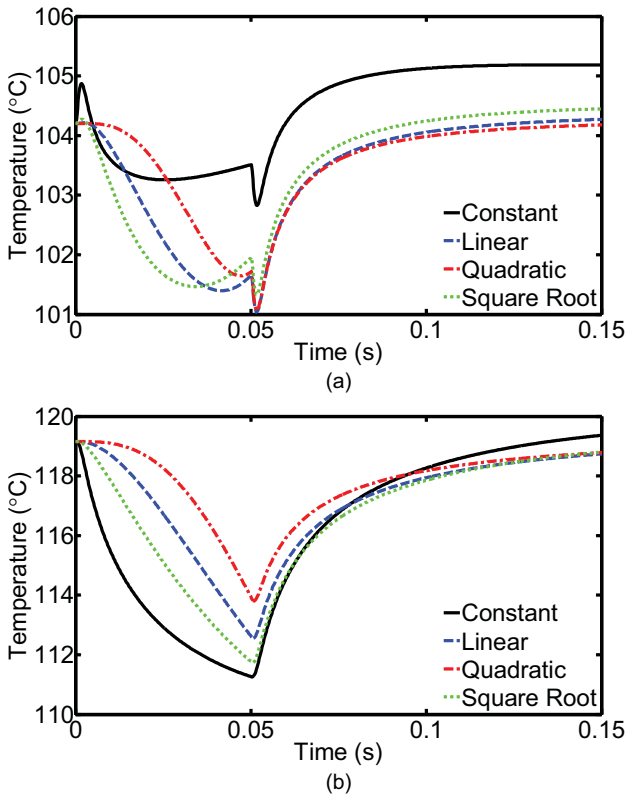


Fig. 13. Hotspot temperature as a function of time with a 0.05 s duration and 8 A pulse applied to the top TEC simultaneously with a 0.05 s duration and 3 A pulse applied to the bottom TEC. Both pulses have the same shape. (a) Temperature of the top hotspot. (b) Temperature of the bottom hotspot.

pulses, reduced top hotspot heating and reduced overshoot make them a good choice for hotspot thermal management of stacked chips.

## VI. Conclusion

A detailed thermal model of a 3-D stacked chip with two dies (top and bottom) and embedded ultrathin ($\sim$100 $\mu$m) TECs was developed. The numerical analysis suggested that TECs can be used for on-demand cooling of hotspots in a 3-D stacked-chip architecture. Passive cooling of up to 9 °C was observed at the hotspot locations on bottom chip without an applied current. Steady-state active cooling caused an additional temperature drop of 5.6 °C because of an applied current in the TEC, which yielded a total of up to 14.6 °C steady-state cooling. A strong vertical coupling was observed between the top and bottom TECs. Thus, bottom TECs can detrimentally heat the top hotspots in both steady-state and transient performance and such configuration should be avoided if possible. Furthermore, the effect of contact resistances was very significant in the stacked-chip architecture and can extensively decrease the COP of TEC devices. It was observed that the TEC-spreader thermal contact resistance can have a dominant effect on TEC performance due to the large magnitude of the TEC-spreader contact resistance compared with the contact resistances inside the TEC module at the thermoelectric-copper interface. Finally, the transient operation of TECs provided more cooling than the steady-state operation. A square root current pulse with 0.05 s duration provided 7.4 °C of active cooling (1.8 °C more cooling than steady state) on the bottom hotspot and used less energy than a constant current pulse. Square root pulses also caused less top hotspot heating than constant current pulses and smaller temperature overshoots. Our analysis showed that TECs can be effective in hotspot thermal management for 3-D packages. However, TECs need to be carefully placed in an electronic package and the applied current through these TECs need to be optimized for an energy-efficient operation. Future developments in the fabrication of ultrathin TEC modules will further encourage efforts on integration of these modules in 3-D packages.

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