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3D Compact Model of Packaged Thermoelectric Coolers

Hotspots on a microelectronic package can severely hurt the performance and long-term reliability of the chip. Thermoelectric coolers (TECs) can provide site-specific and on-demand cooling of hot spots in microprocessors. We develop a 3D compact model for fast and accurate modeling of a TEC device integrated inside an electronic package. A 1D compact model of a TEC is first built in SPICE and validated for steady-state and transient behavior against a finite-volume model. The 1D compact model of the TEC is then incorporated into a 3D compact model of a prototype electronic package. The results from the compact model for the packaged TEC are in good agreement with a finite-volume based model, which confirms the compact model's ability to accurately model the TEC's interaction with the package. Analysis of packaged TECs using this 3D compact model shows that (i) moving TECs closer to the chip results in faster response time and an increase in maximum cooling, (ii) high thermal contact resistance within the thermoelectric cooler significantly degrades performance of the device, and (iii) higher convective heat transfer coefficients (HTC) at the heat spreader surface increase steady-state cooling but decrease maximum transient cooling. [DOI: 10.1115/1.4024653]

Keywords: thermoelectric, compact model, TIM, heat transfer coefficient

1 Introduction

Effective cooling of microelectronic processors is a crucial area of microelectronics research as packages decrease in size and volumetric heat generation within these packages increase drastically. High heat flux areas (∼hot spots) on the chip can detrimentally affect the performance and must be effectively cooled in order to provide prolonged operation time of chip and less frequent throttling of the processor speeds [1–3]. Conventional cooling techniques are capable of removing high heat fluxes but are unable to provide localized cooling of hot spots and are therefore inefficient for heat removal from hot spots [1]. Thermoelectric coolers can be an effective solution as they provide site-specific and on-demand cooling, which can prolong the use of the chip in both a short term boost of processing speeds as well as a long-term boost in chip reliability [4–7].

Thermoelectric coolers are reliable and easy to maintain with no moving parts, but they are limited by their low efficiency and low heat flux pumping capability. Thermoelectric coolers are generally compared using the thermoelectric figure of merit $ZT = S^2\sigma T/k$, where S is the seebeck coefficient, T is the absolute temperature, and σ and k are electrical and thermal conductivities, respectively [8]. Thermoelectric coolers made of Bi_2Te_3 have recently been incorporated in an electronic package with total cooling up to 15 °C at the hot spot [1]. TECs can be used for both steady-state and transient cooling of hotspots. Previous works have studied both the steady-state and transient behavior of thermoelectric coolers in detail [9–13]. These studies found that pulsed current through TECs could result in additional cooling during transient operation above the cooling achieved during steady-state operation, because the peltier cooling takes effect before the Joule heating is realized at the cold junction [9–11]. Our previous works have simulated TECs in an electronic package using a finite-volume based computational method [12,13]. These simulations provided results which are in good agreement with experimental results in Ref. [1] but the simulations took a considerable amount of computational time, especially the transient simulations, and thus did not allow for extensive variation of the parameters involved. A compact model of the TEC device allows for easy input into a variety of package models leading to rapid analysis and design.

Compact models of thermoelectric coolers have been presented in the previous studies. A detailed SPICE model of an isolated single TEC is presented in Refs. [14,15]. Individual n-p poles are modeled to simulate the physics of the thermoelectric material itself, but the model considers only the thermoelectric material; it does not include the effect of contact resistances and has not been incorporated within a larger package. Another model of a TEC has been presented in Ref. [16] using the framework of MATLAB and its Simulink tool. This model is based on the SPICE tool outlined in Ref. [14,15], but is intended to easily integrate with the existing control schemes employed in MATLAB and Simulink. A 3D compact model of TECs integrated into a microelectronic package has not been developed for performance analysis of packaged TECs. The geometrical and thermal properties of different materials of an electronic package, such as the thermal interface material (TIM), heat spreader, and heat sink, and the attached cooling solutions significantly affect the performance of TECs. The previous models of isolated TECs can analyze the effect of different TE material properties used in the TEC module, but a model of the entire package, with embedded TECs, is required to investigate the real operation of TECs in electronic packages, compare against experiments, and optimize the TECs' performance.

The present work develops a 3D compact model of an electronic package with embedded TECs for rapid analysis of Peltier cooling at hotspots inside a chip. This paper first outlines the development and validation of a 1D compact model in both steady-state and transient operation (Sec. 2). Next, this compact model of TEC is integrated into a 3D compact model of a prototype package showing the utility and ability of the model to perform rapid analysis of Peltier cooling inside a package (Sec. 3). The effect of proximity of the thermoelectric cooler to the top of the chip, the effect of thermal contact resistance inside the TEC on the TEC's performance, and the effect of the convective heat transfer coefficient imposed at the top of the heat spreader on the TEC's performance have been investigated in Sec. 4. These simulations further confirm the capability of the model to investigate the effect of a TEC's environment on TEC operation in a

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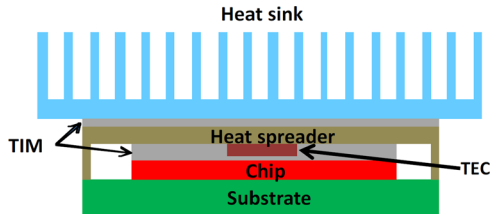

Fig. 1 Schematic of the electronic package with integrated TEC

Table 1 Material properties and dimensions of different components of the electronic package

Component	Thermal conductivity (W/m K)	Specific heat (J/kg K)	Dimensions
Spreader (Cu)	400	381	23 mm × 1 mm × 23 mm
TIM	1.75	700	9 mm × 0.124 mm × 9 mm
TEC-superlattice	1.2	16	3 mm × 0.008 mm × 3 mm
Chip (Si)	140	712	9 mm × 0.5 mm × 9 mm

computationally efficient manner with sufficient accuracy. Finally, Sec. 5 concludes the paper.

2 Development and Validation of TEC Compact Model

The thermal model of an electronic packaging with thermoelectric cooler was first developed using commercial CFD package FLUENT and the meshing software GAMBIT. The model solves Fourier's conduction equations for the electronic packaging and TEC module and provides temperature distributions for the entire package. The present work considered a TEC module with 49 p-n couples arranged in a 7×7 array within a 3.0 mm × 3.0 mm TEC device. The 8 μm thick Bi_2Te_3 superlattice material is used as TE material, which is sandwiched between two 46 μm metallic layers on either side, making the TEC device 100 μm thick. The computational domain of the thermal FLUENT model included heat spreader, TIM, chip, and TEC. The heat sink was modeled as a convective boundary condition at the top surface of the heat spreader with a convection heat transfer coefficient, h, of 2050 W/m^2. A schematic of the geometry used in the FLUENT model is shown in Fig. 1.

This geometry was chosen as it allowed the model to be validated against the steady-state experimental and computational results presented in Ref. [1]. Material properties for the various components of the electronic package are listed in Table 1. The electrical/thermal contact resistances at the interface of the superlattice-metal layer (10^{-11} Ωm^2; 10^{-6} m^{2}K/W) inside TEC device and at the interface of the TEC device—heat spreader layer (8×10^{-6} m^2 K/W) were also taken from Ref. [1]. The chip has a uniform heat flux of 43 W/cm^2.

The Peltier cooling by the TEC device was incorporated by adding heat ($\sim SIT_h$) at the hot side and subtracting heat ($\sim SIT_c$) from the cold side of the superlattice, where T_h and T_c are the temperatures of the hot and cold sides, respectively. The value of S was taken to be 300 μV/K based on the experimental measurements in Ref. [1]. The heat generation due to the electrical resistance of the thermoelectric material and the contact resistances at the interface of superlattice-metal layer inside device was considered by adding an I^2R term at the corresponding volumes and layers. The thermal contact resistances at these interfaces were considered by adding appropriate thermal resistance at the interfaces. In our previous work [12], we compared the finite-volume model developed in FLUENT to the numerical results of Ref. [1] which were verified against the experimental results of Ref. [1]. Excellent agreement between the results of Ref. [1] and the FLUENT model (within 2–3 °C) validated the finite-volume model and also provided a reference finite-volume model to compare and validate the compact models of packaged TECs developed in the present work.

A compact 1D resistor model is first developed in SPICE for an isolated TEC subjected to heat flux on one side and convective cooling on the other side. A 1D finite-volume based model using FLUENT is also created for comparing against the results obtained from the 1D resistor network model in SPICE. The "one-dimensional" FLUENT model consisted of the same layers and contact resistances inside the TEC module as the previous full TEC-package FLUENT model, but the model consists only of the area of a single TEC of lateral dimensions, 3 mm × 3 mm. The FLUENT model is essentially a 1D model as the vertical surfaces of TEC module were insulated and there is no lateral thermal spreading, which is confirmed by observing the constant temperature distributions in several horizontal slices.

The 1D compact model of a TEC is developed following the geometry of the FLUENT model in order to ensure significant agreement between the two models. The compact model is constructed in SPICE and provides a thermal resistor network that can be solved

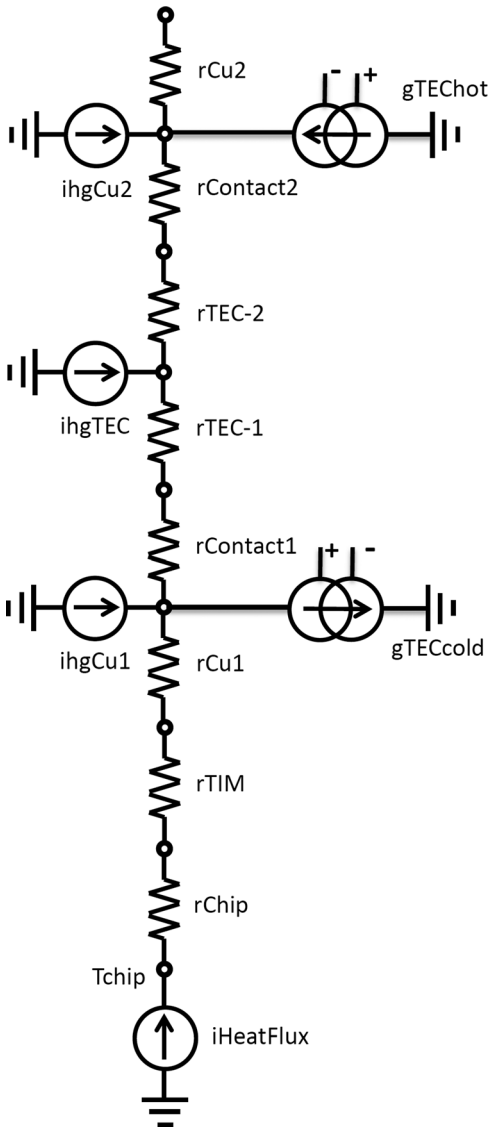

Fig. 2 One-dimensional steady-state compact model of the thermoelectric cooled integrated inside package; top node of TEC connects to the ambient through a heat spreader

Table 2 Summary of elements in 1D compact model

Element name	Function
rCu2	Top copper layer of TEC device
ihgCu2	Current source representing electrical contact resistance between copper and Bi_2Te_3 superlattice
gTEChot	Adds heat to top of superlattice layer $\propto SIT_{hot}$
rContact2	Top thermal contact resistance between copper and Bi_2Te_3 superlattice
rTEC-2	Superlattice layer of TEC device
ihgTEC	Heat dissipation within TEC device
rTEC-1	Superlattice layer of TEC device
rContact1	Bottom thermal contact resistance between copper and Bi_2Te_3 superlattice
ihgCu1	Current source representing electrical contact resistance between copper and Bi_2Te_3 superlattice
gTECcold	Removes heat from bottom of superlattice layer $\propto SIT_{cold}$
rCu1	Bottom copper layer of TEC device
rTIM	Thermal resistance of thermal interface material between chip and TEC device
rChip	Thermal resistance of silicon chip material
Tchip	Temperature of bottom of silicon chip
iHeatFlux	Power source at bottom of chip

using circuit analysis techniques. The one-dimensional steady-state compact model can be seen in Fig. 2 and consists of resistors, current sources, voltage sources, and voltage controlled current sources. The resistors represent different materials as well as the thermal contact resistances inside the TEC device and at the TEC-spreader interface in FLUENT model. The current sources simulate the chip heat flux at the bottom surface (iHeatFlux) as well as electrical heat generation that occurs in the TEC due to a current being passed through the device. The last elements are the voltage controlled current sources or G-elements, which represent the cooling effects of the TEC by removing heat at the cold surface (gTECcold) and adding heat at the hot surface (gTEChot), depending on the temperature difference between the two sides. The cold side of TEC is being actively cooled (heat is removed) and the heat is rejected at the hot side. The top of the model shown in Fig. 2 connects to a heat spreader made of copper which is connected through a convective resistance to a voltage source for simulating the effect of the convective boundary condition and ambient temperature. No spreading resistance is needed between the TEC and heat spreader, because the 1D compact model is being compared with a 1D FLUENT model that has no lateral spreading effects. All elements of the compact model shown in Fig. 2 are outlined in Table 2 with descriptions of their function within the model.

The thermal resistance values for different conductive and convective element were calculated using Eq. (1)

$$R_{\text{conduction}} = \frac{L}{kA} \quad \text{and} \quad R_{\text{convection}} = \frac{1}{hA} \tag{1}$$

Here, L is the thickness of the material, k is the thermal conductivity of the material, A is the cross-sectional area of the element, and h is the convection coefficient. When the model is converted to a transient model, thermal capacitance is included for each material layer, which consists of a capacitor with a capacitance (C) calculated as, $C = \rho c_p$. Here, ρ is the density of the material and c_p is the specific heat of the material. The units of resistance and capacitance are K/W and J/m^3 K, respectively.

The 1D compact model is validated against the 1D FLUENT model for both steady-state and transient behavior. All elements in the compact model had area of 3 mm × 3 mm, which is same as the TEC area used in the FLUENT model. The steady-state validation of the 1D compact model against the 1D finite-volume model can be seen in Fig. 3. Temperatures at the bottom of chip (source of heat flux), bottom of TEC superlattice (cold side), and top of TEC superlattice (hot side) are compared. The results are comparable and follow similar trends. Figure 4 shows the relative error in percentage. The error grows as the current is increased, but the error is below 2% for the range of the current amplitudes that will be considered within this work and for the typical TEC operation. This means that the compact model is capable of providing results very similar to the finite-volume method.

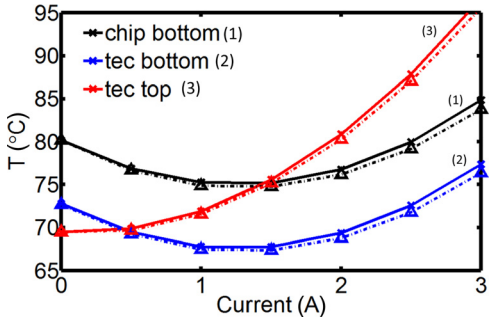

Fig. 3 Steady-state validation of the 1D compact model (dashed lines) against the 1D finite-volume model (solid lines) at varying current. Temperatures at bottom of chip (source of heat flux), bottom of TEC superlattice (cold side), and top of TEC superlattice (hot side) are compared.

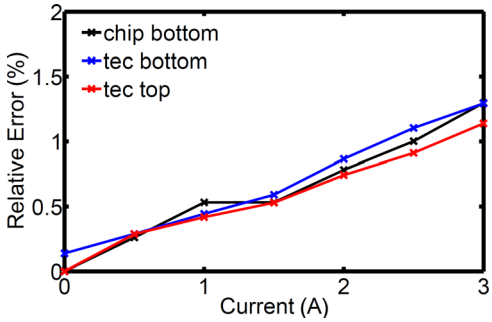

Fig. 4 Relative steady-state error between the finite-volume model and compact model for various currents

The model is then validated for the transient behavior considering the thermal capacitance of different components; the comparison of finite-volume method to compact model is shown in Fig. 5. Once again the 1D finite-volume model and 1D compact model follow similar trends. The relative error of the compact model compared to the finite-volume method is shown in Fig. 6. The error grows with increasing current similar to the steady-state models, but even with 8 A of current the maximum error is below 2.5% and further decreases with time. The transient results for hot spot temperature from the compact model were in good agreement with the finite-volume based model results. This close agreement of compact model with finite-volume method based model in both steady-state and transient operation, suggests that the compact model can be used as an alternate model for all further simulations.

Section 3 outlines the inclusion of the TEC model into a 3D compact model of the chip package and provides simulation time comparisons which shows the superiority of the compact model for rapid modeling and analysis of packaged TECs.

3 Modeling of TEC Integrated Inside an Electronic Package

The compact model of the TEC device is integrated into a 3D electronic package compact model for further simulations.

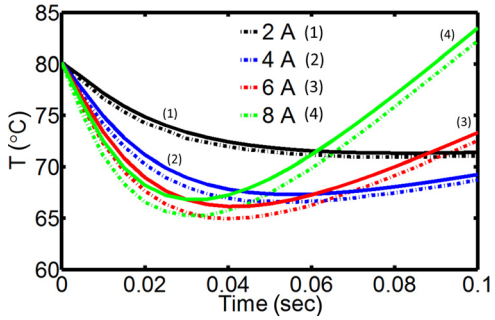

Fig. 5 Validation of the transient temperature behavior obtained from 1D compact model (dashed lines) against the 1D finite-volume model (solid lines) at varying currents; temperature is measured at the bottom of chip

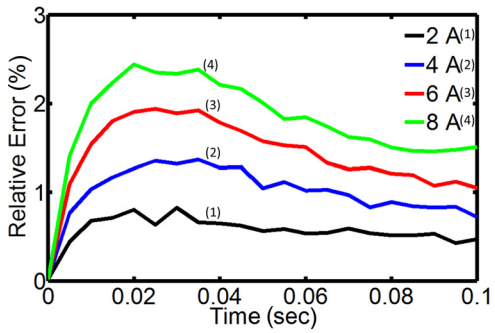

Fig. 6 Relative error for time varying peak temperature at the bottom surface of the chip computed from the finite-volume method and compact models at various currents

The package has a 9 mm × 9 mm chip with a 3 mm × 3 mm TEC device placed at the center. A heat flux boundary condition (∼427,000 W/m^2) is applied at the bottom surface of the chip, making the chip power approximately 35 W. The thickness of the heat spreader, TIM, and chip were considered as 1 mm, 0.125 mm, and 0.5 mm, respectively. The resistor–capacitor configuration of a single cell in the chip package can be seen in Fig. 7. The chip package is built using thousands of these cells, each belonging to one of the three package materials: silicon for the chip, thermal interface material for the chip-spreader interface, or copper for the heat spreader. The TEC compact model is inserted within the chip package model as a subcircuit consisting of the resistor network from rCu1 to rCu2 in Fig. 2, and each instance of the TEC only needs two nodes to connect to the package model. The model is easily adaptable to changes in grid size; a grid-independence test was completed and it was observed that 0.5 mm × 0.5 mm lateral gridding was sufficient for further simulations.

The package and TEC model consists of many vertical 1D resistor networks connected by a 2D resistor array in order to create a 3D package. Spreading resistance is not included because the model is capable of modeling lateral spreading throughout the geometry due to the 3D resistor connections between nodes. The developed 3D compact model considers the heat spreader lateral dimensions similar to the chip dimensions, i.e., 9 mm × 9 mm. In order to consider the effect of a large heat spreader (> 9 mm × 9 mm), equivalent resistors were added to all sides of the heat spreader to simulate convection and spreading that would occur if a larger heat spreader were present. The largest heat spreader size considered in the present work is 23 mm × 23 mm, which is according to the geometry specified in Ref. [13]. The extension of the heat spreader along all four sides is assumed to be a straight rectangular fin extending out from the 9 mm × 9 mm spreader with the equivalent resistance, R_{fin}, estimated using Eqs. (2)–(4) described below [17,18]

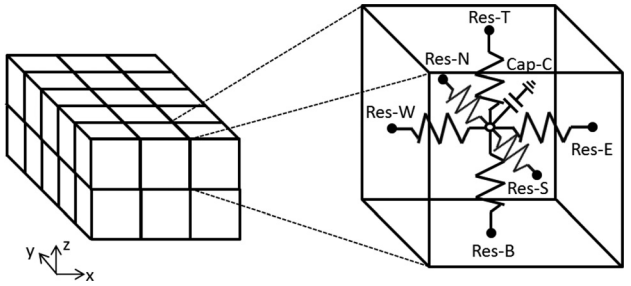

Fig. 7 Sample "mesh" and the accompanying resistor–capacitor network model for a single cell of chip or electronic package (∼chip, TIM, or heat spreader); abbreviations stand for north (N), south (S), east (E), west (W), top (T), bottom (B), and center (C)

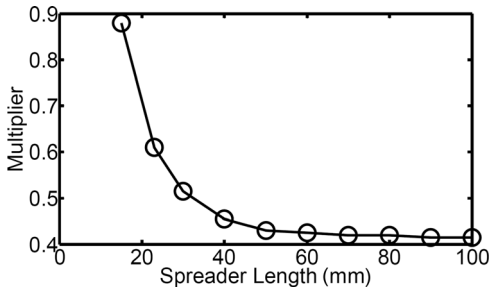

Fig. 8 Multiplier for additional resistance of larger heat spreader versus spreader length (mm)

$$R_{fin} = \frac{1}{hA_f\eta_f} \tag{2}$$

$$\eta_f = \frac{\tanh(mL_c)}{mL_c} \tag{3}$$

$$m = \sqrt{\frac{hP}{kA_c}} \tag{4}$$

The equivalent resistance of the fin, R_{fin}, is a function of h, A_f, and η_f, where h is the convective heat transfer coefficient, A_f is the surface area of the fin, and η_f is the fin efficiency defined by Eq. (3). The fin efficiency, η_f, is a function of L_c and m, where L_c is the characteristic length and m is defined by Eq. (4). m is a function of h, P, k, and A_c, where P is the perimeter of the fin, k is the conductivity of the fin material, and A_c is the cross-sectional area of the fin. The equivalent resistance values of the fins need to be calibrated against the results from the FLUENT model, i.e., a multiplier is needed to correct R_{fin} as the FLUENT model considers convection on only one side of the fin, whereas the equivalent resistance model considers both sides of the fins. In addition, the equivalent resistances added to the compact model only consider fins projecting straight from the four sides of the spreader, and do not model the corner areas of the heat spreader. The compact model is in good agreement with FLUENT results for both steady-state and transient simulations if the resistance of the fin is multiplied by a derived constant (∼multiplier), which varies with the equivalent size of the heat spreader. The multipliers are plotted against spreader size in Fig. 8. The multipliers varied from 1 to 0.4; the limits correspond to a heat spreader of the same size as the chip and to a very large heat spreader, respectively. The multiplier appears to saturate to 0.4 at large heat spreader size as further increase in heat spreader size does not lead to any additional effective cooling of the system.

The steady-state and transient comparisons are shown in Figs. 9 and 10, respectively. The compact model's steady-state and transient behavior are very close to the finite-volume model.

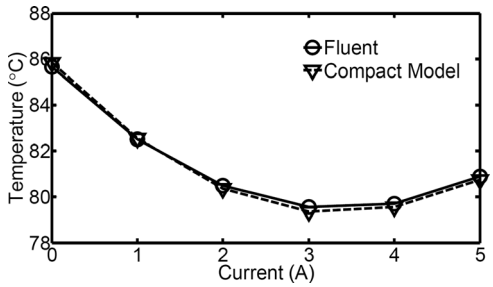

Fig. 9 Steady-state validation of the compact model of TEC integrated inside an electronic package (using equivalent spreader resistance (dashed line) against finite-volume model (solid line) at various currents. The comparison is done for temperature at the center of the chip, directly below the location of TEC.

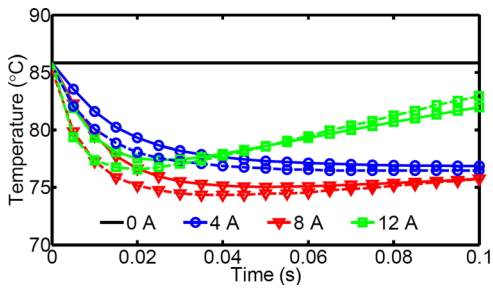

Fig. 10 Transient validation of the compact model of TEC integrated inside an electronic package (using equivalent spreader resistance; dashed lines) against the finite-volume model (solid lines) for currents varying from 0 A to 12 A. The comparison is done for temperature at the center of the chip, directly below the location of TEC.

The addition of the spreader equivalent resistors and use of the multiplier has reduced the steady-state error dramatically (maximum relative error of ~0.019%). The error present during the transient operation (maximum relative error of ~2.9% for 8 A current) is also within the acceptable ranges and validates the applicability of the compact model. The transient behavior of the package with the integrated TEC device at various currents is shown in Fig. 10. The temperatures in this figure correspond to the center of the bottom surface of the chip, directly below the center of the TEC device. The optimal current for transient behavior is observed to be 8 A for the package geometry considered in the simulations and results in approximately 12 deg of cooling in the package. Increasing the amplitude of the transient current pulse results in an increase in cooling with a shorter response time, but the cooling lasts for shorter amounts of time as the current amplitude is increased. This is due to the Peltier cooling at surface which has faster response than the volumetric Joule heating within the TEC device. For current pulses with higher amplitudes, the Joule heating increases rapidly ($\sim I^2$) and overcomes the Peltier cooling provided by the TEC device. Four amps current pulse takes approximately 0.1 s to reach maximum cooling, but 12 A current only takes 0.02 s to reach maximum cooling. TEC controllers should be able to detect the temperature rise at a hot-spot and turn on a TEC for appropriate periods of time and current amplitudes in order to properly react to the thermal needs of the package. The computational time for the results shown in Fig. 10 with 12 A current was estimated. The FLUENT model took 674.3 s, whereas the SPICE model took 156.34 s; a 430% reduction in computation time.

4 Results and Discussion

In this section, we use the developed compact model of packaged TECs to analyze the hot spot cooling on chip. We investigate

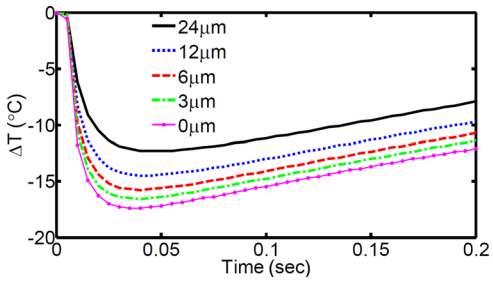

Fig. 11 Effect of thickness of TIM material between chip and bottom of TEC device on the transient behavior of the TEC device with a current of 8 A; five thicknesses are tested: 24 μm, 12 μm, 6 μm, 3 μm, and 0 μm

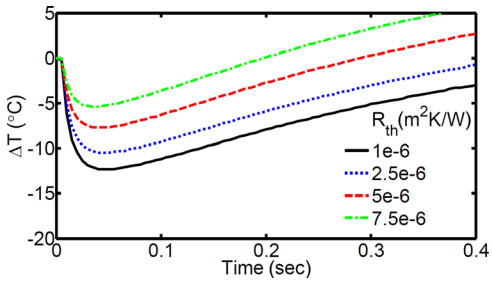

Fig. 12 Effect of thermal contact resistance within TEC on transient performance of the TEC device for various thermal contact resistances between copper and superlattice layers and constant TEC current of 8 A; thermal contact resistances are in the range of 1×10^{-6}–7.5×10^{-6} m^2 K/W

the effect of TEC location with respect to the chip, the effect of thermal contact resistances inside TEC device, and the effect of cooling solution attached with the package on Peltier cooling by TEC. The hot spot (500 W/cm^2) is placed at the center of bottom surface of chip with an area of 1 mm × 1 mm, while the rest of the chip still has a heat flux of 43 W/cm^2.

4.1 Effect of TEC Location. In this section, we investigate the effect of TEC location inside the package on TEC performance using the compact model developed in Sec. 3. The focus of this investigation is to evaluate how the location of the device affects the device performance and degree of cooling at hot spots. We recognize that manufacturing constraints exist in placing a TEC device inside the package. In the model used for the results in Fig. 10, a 24 μm thick TIM layer exists between the top of the chip and the bottom of the TEC device. Figure 11 shows the effect of decreasing this thickness from 24 μm to 0 μm, which is effectively decreasing the thermal resistance and capacitance between the chip and TEC device to zero. The degree of cooling achieved by the TEC device is higher and the maximum cooling occurs faster as the thickness of the TIM is decreased, effectively decreasing the response time of the TEC device for cooling the chip. Since the thermal resistance of any material is proportional to L/k, it can be expected that the results of Fig. 11 would occur with a proportional increase in the conductivity of the TIM as well. Therefore, either a decrease in TIM thickness between the top of the chip and bottom of the TEC device or an increase in the TIM conductivity by use of a different material can result in faster and better control of temperatures on chip while using a TEC device.

4.2 Effect of Thermal Contact Resistance. As seen in Ref. [13], thermal contact resistances within the TEC can have detrimental effects on the behavior of the TEC device. Figure 12 shows the performance of the compact model for increasing the

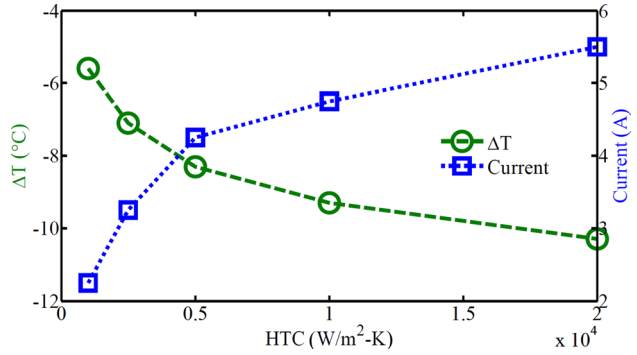

Fig. 13 Maximum steady-state cooling and associated currents for various HTC at top surface of heat spreader; HTC is varied in the range of 1000 W/m^2 K to 20,000 W/m^2 K

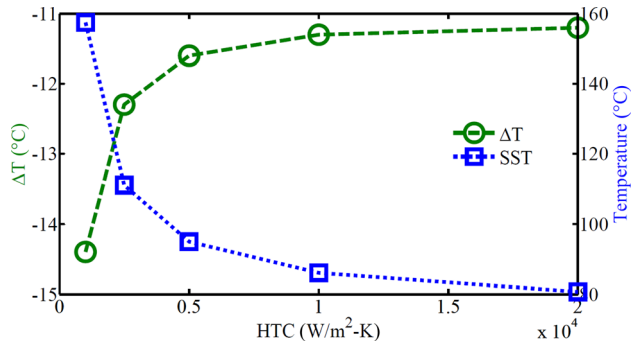

Fig. 14 Maximum transient cooling (ΔT) and steady-state temperature (SST) with zero TEC current for various heat transfer coefficients at top surface of heat spreader, varying from 1000 W/m^2 K to 20,000 W/m^2 K; maximum cooling occurred at 7.5 A and 0.045 s for all cases

thermal contact resistance between the copper and superlattice layers from 1×10^{-6} to 7.5×10^{-6} m^2 K/W. It is expected that the cooling provided by TEC device will degrade as the thermal contact resistance within the TEC increases. The compact model provides the expected results, i.e., cooling decreases as the thermal contact resistance increases. When contact resistance is increased from 1×10^{-6} to 7.5×10^{-6} m^2 K/W, the cooling at hot spot degrades from 12 deg to 5 deg which is over 50% reduction in the cooling performance of the TEC device. This result emphasizes the importance of the quality of the interfaces inside TEC device. Depending on the fabrication method of the TEC modules and materials used in TEC device, the quality of interfaces can significantly change and an interface with high thermal contact resistance can severely hamper the TEC's ability to perform.

4.3 Effect of Cooling Solution. The HTC is typically employed at the top of the heat spreader to represent cooling by attached heat sink and the fluid flow through heat sink. The material, design and size of the heat sinks and the mass flow rate of the fluid through the heat sink affect the total amount of heat which can be removed using such cooling solution. The effective HTC applied at the top side of the heat spreader can significantly affect the TEC's performance. Figure 13 depicts the effect of varying HTC on the maximum steady-state cooling of the TEC and the current amplitude at which this maximum cooling occurs. The heat transfer coefficient is varied from 1000 W/m^2 K to 20,000 W/m^2 K, which represents a wide range of cooling solutions that can be employed for heat removal from microelectronic packages [17]. The maximum Peltier cooling obtained by using TECs at steady-state significantly increases for HTC in the range of 1000–5,000 W/m^2 K. The Peltier cooling on chip approaches saturation with further increases in HTC or convective cooling. The point of saturation is due to the convective resistance approaching zero relative to other resistances in the system such as the conductance resistance of materials or contact resistances at interfaces. The results in Fig. 13 correspond to the materials and size of the electronic package under consideration, but similar trends are expected for other chip packages. The current associated with maximum cooling is also specified for each HTC considered and appears to follow a similar trend, i.e., the current amplitude for maximum cooling increases and approaches to saturation after 5000 W/m^2 K. The analysis emphasizes that better cooling solutions used for the microelectronic package will also lead to the enhanced capability of TECs in cooling hot spots on the chip.

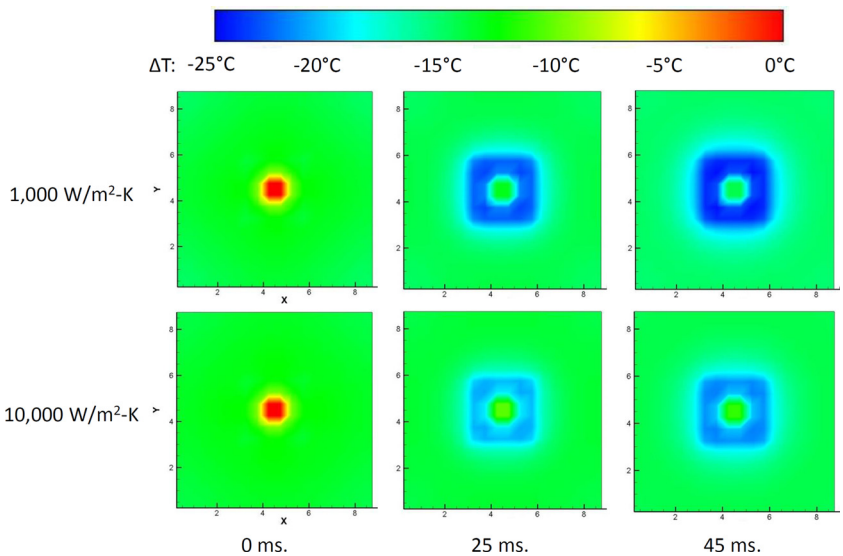

Fig. 15 Contour plots of ΔT_p at the bottom surface of chip, using the 3D compact model, for convective heat transfer coefficients 1000 W/m^2 K and 10,000 W/m^2 K at three different time steps: 0 ms, 25 ms, and 45 ms. Here, for each convection coefficient, ΔT_p is estimated as temperature difference with respect to the peak temperature on chip at $t = 0$ ms.

We next analyze the effect of HTC on the transient operation of packaged TECs. Figure 14 shows the steady-state temperature (SST) at hot spot for various heat transfer coefficients when no current is applied through TECs and the maximum Peltier cooling at hot spot (ΔT) during transient operation of TECs using a current pulse of 7.5 A. The maximum cooling occurred at 7.5 A and 0.045 s for the entire range of HTCs considered, so the heat transfer coefficient had no effect on the optimal current or response time for the transient cooling. The maximum transient cooling decreases from 14.4 °C to 11.2 °C as the HTC increases from 1000 W/m^2 K to 20,000 W/m^2 K, which is in stark contrast with the steady-state cooling results. This can be explained by SSTs plotted in Fig. 13 for different HTCs. As the HTC is increased, the steady-state temperature decreases rapidly and then saturates to constant values as the convective resistance essentially approaches zero in comparison to the rest of the system. Increasing HTC at spreader surface leads to a different temperature distribution in the electronic package and reduces the hot spot temperature at steady state. The high HTC coefficient does not help improve heat removal from TEC hot side in transient operation, which is reflected in the same optimal current for maximum cooling and the same time to achieve this maximum cooling for the entire range of HTCs considered. However, the lower steady-state temperature at hot spots for high HTC leads to less cooling by TECs (ΔT in Fig. 14) during transient operation; this behavior is further supported by observing the similar trend of saturation with HTC for both SST and ΔT in Fig. 13. Contour plots of ΔT_p for the transient simulations are shown in Fig. 15 for HTC 1000 W/m^2 K and 10,000 W/m^2 K and for three different time steps: 0 ms, 25 ms, and 45 ms. Here, ΔT_p represents the difference in temperature as compared to the peak temperature on chip at $t = 0$ ms for a given HTC. The peak temperature on chip varies with HTC as shown in Fig. 13, but such representation of ΔT_p provides a good way of comparing the contour plots for different HTCs. As shown, the lower HTC corresponds to higher Peltier cooling under the TEC at different time instants, which could be due to the elevated steady-state temperature of the hot spot on chip with a lower HTC as discussed above.

5 Conclusion

In summary, a compact model of a TEC was developed and validated for 1D steady-state and transient behavior against a detailed 1D finite-volume model. The compact model of TEC was then integrated into a 3D compact model of a chip package. This 3D compact model can simulate the response of a packaged TEC in significantly reduced time with reasonable accuracy when compared to the 3D finite-volume based model; in one scenario the computation time was reduced by 430%. Investigation of the packaged TEC using the compact model suggests that the TEC provided optimal cooling with a current of 8 A during transient operation. The degree of cooling and response time improved as the thermoelectric cooler was moved closer to the top of the chip. Increasing the thermal contact resistance at metal-TE material interface within the TEC device detrimentally hurt its performance. Increasing the heat transfer coefficient at the top surface of the heat spreader results in an increase in maximum steady-state cooling but decreases the maximum transient cooling. Future work will consist of further exploration of different electronic packages and design of an efficient and realistic controller.

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