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On-Chip Power Generation Using Ultrathin Thermoelectric Generators

Thermoelectric generators (TEGs) can significantly improve the net power consumption and battery life of the low power mobile devices or high performance devices by generating power from their waste heat. Recent advancements also show that the ultrathin thermoelectric devices can be fabricated and integrated within a micro-electronic package. This work investigates the power generation by an ultrathin TEG embedded within a micro-electronic package considering several key parameters such as load resistance, chip heat flux, and proximity of the TEG to chip. The analysis shows that the power generation from TEGs increases with increasing background heat flux on chip or when TEGs are moved closer to the chip. An array of embedded TEGs is considered in order to analyze the influence of multiple TEGs on total power generation and conversion efficiency. Increasing the number of TEGs from one to nine increases the useful power generation from 72.9 mW to 378.4 mW but decreases the average conversion efficiency from 0.47% to 0.32%. The average power generated per TEG gradually decrease from 72.9 mW to 42.0 mW when number of TEGs is increased from one to nine, but the total useful power generated using nine TEGs is significant and emphasize the benefits of using embedded TEGs to reduce net power consumption in electronics packages. [DOI: 10.1115/1.4027995]

Keywords: thermoelectric generators, harvesting, waste heat, embedded, Seebeck coefficient

1 Introduction

TEGs produce an electromotive effect, known as the Seebeck voltage, when a temperature difference is applied across the two ends of the device. TEGs have been used on spacecraft to provide an energy source millions of miles away from the Earth's surface [1]. This is an extreme case where other energy sources may not be available. TEGs have also been widely used to generate power for remote data communication system used in oil and gas pipelines and for polar weather stations [2]. Some studies have also delved into the possible use of TEGs in automobile exhaust pipes to reduce the load on a vehicle's alternator [3]. Recently, the possibility of humans wearing TEGs to power various biomedical sensors has been explored [4]. There are many possible applications of TEGs but improving the efficiency of TEGs is still the biggest challenge which is required to be overcome to make these devices cost-effective and attractive solution as a green and commercially viable technology. Suitable materials which can provide optimized properties (i.e., very low thermal conductivity, very high electrical conductivity, and high Seebeck coefficient) for high figure of merit are being explored with some promising candidates already discovered but more work is still required [5]. One of the interesting applications is to embed TEGs inside an electronic package for energy harvesting from chip waste heat. Embedded TEGs can reduce the net power consumption of a chip, but this important application of TEGs is relatively less explored and focus of the present study.

Besides the material properties, temperature difference across the TEG also determines its efficiency. Different TEG materials

obtain their optimum efficiency in different temperature regimes, and therefore different applications may require different TEG materials depending upon the available temperature difference. Crane et al. built a generator consisting of many smaller TEGs and demonstrated 130 W of power generation from a 205 °C temperature difference [6]. This is a significantly large power output by a TEG, but such large temperature difference is not available in most scenarios. Small temperature differences are available across many electronic devices, which can be used to harvest energy by TEGs to enhance the overall energy efficiency of the system. Solbrekken et al. attached 1 mm thick TEGs to a portable device's central processing unit (CPU) and powered a fan using available temperature difference of approximately 30 °C to generate 40–50 mW of power [7]. The fan was able to keep the CPU temperature below 85 °C in a 35 °C ambient environment [7]. This hybrid cooling solution harvests energy from the waste heat and power a fan to remove heat from the package, turning an active form of cooling into a passive form since it no longer requires a battery to power fan [7]. The power generated by TEGs can also be used to assist the power source of micropumps for microchannel cooling of electronic packages [8–10]. If the TEGs can be moved closer to heat dissipating elements, higher power can be harvested, e.g., embedding TEG inside the package. However, the integration of TEGs inside the package can be challenging for high performance computing or mobile technologies. Particularly, 1 mm thick TEGs are too thick to be embedded inside electronic packages. Bi₂Te₃ superlattice based thermoelectric cooler (TEC) has been fabricated and integrated within an electronic package by Chowdhury et al. [11]; this TE device is thin enough (~100 μm) to be embedded within a typical micro-electronic package [11].

Bi and Te based TE materials have high figure of merit at room temperature and so they are one of the best TE materials for hot spot cooling inside or energy harvesting from a micro-electronic

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package [12,13]. The Bi_2Te_3 superlattice based ultrathin TECs showed increased performance compared to the TECs made by other materials [11]. Bi_2Te_3 based TE devices can be fabricated using standard semiconductor manufacturing techniques, which allows these devices to be relatively easily integrated within a package [14]. Use of standard semiconductor manufacturing tools allows scaling of the devices to cater to the power generation need of a particular device, e.g., from simple modules providing a few milliwatts to interconnected module-arrays providing tens of watts [13]. Some recent research has investigated the possibility of using silicon nanowires as potential TE material [15]. Silicon is poor thermoelectric material in its bulk form, but the figure of merit of rough silicon nanowires (~ 1) can be two orders of magnitude higher than bulk Si (~ 0.01) [15]. Li et al. fabricated silicon nanowire based TEGs, which has footprint of $5\text{ mm} \times 5\text{ mm}$ consisting 162 thermocouples, and generated 1.5 nW with a 0.12 K temperature difference [15]. Silicon nanowires based TEGs are CMOS compatible compared to the Bi, Te, Sb, and Se based TEGs and thus could be integrated much closer to the electronic circuitry [15]. However, the power generation by silicon nanowire based embedded TEGs is still very low and significant work is required to improve its efficiency. Bi_2Te_3 based TEG seems more promising and hence chosen for investigation by the present work.

Some studies focused on power generation using TEGs attached to a micro-electronic package [6,7,16–19], but the investigation of power generation using Bi_2Te_3 based ultrathin TEGs embedded within an electronic packaging has not been addressed. Gould et al. integrated a TEG on a desktop computer's CPU and attached a heat sink to the other side of the TEG [20]. This TE device generated power in the range of hundreds of microwatts to few milliwatts [20]. The temperature difference across the device is very low ($\sim 2^\circ\text{C}$) as it was integrated outside the electronic package [20]. Embedding a TEG inside an electronic package, closer to the heat source can provide larger temperature differences across its TE element. Most of the previous models of the TEGs consider constant temperatures at the hot and cold junctions [6,16–19]. Constant temperatures at the two junctions of the TEGs is applicable in only few situations, e.g., fluid flow on both sides of a TEG with different temperatures [18]. For embedded TEGs, the package environment can significantly affect the power generation and efficiency of TEGs. So, it is crucial to consider the effect of the structure and properties of packaging materials and the boundary conditions. Several recent works have suggested that maximum power generation in complex systems corresponds to the case when the load resistance is greater than the device resistance rather than when they are equal [7,21]. This deviation from the expected behavior occurs if the temperatures of the junctions are not kept constant, and such a situation is more realistic and applicable for a larger set of scenarios including embedded TEGs. It is important to analyze the optimum load resistance for power generation by TEGs embedded inside a package that has no constant temperature boundaries. This is addressed in the present study.

In our previous work [22,23], we have developed numerical model of a package with embedded TECs. The dimensions and properties of these devices are similar to the devices fabricated by Chowdhury et al. [11]. The present work builds on these previous models to explore the possibility of using packaged thin-film superlattice based TE devices as TEGs. The goal of the present work is to investigate the power generation by Bi_2Te_3 superlattice based TEGs embedded inside an electronic package. This work first outlines the development of the 3D numerical model of the package and multiple embedded TEGs for a steady-state operation. Section 4 presents an analysis of one TEG located at the center of the package and decipher the effect of key parameters: load resistance, background heat flux, and proximity of TEG to chip on power generation. Then, multiple TEGs are added to the package and comparison of various configurations of TEGs is performed to explore the power generation capability and efficiency of array of embedded TEGs. Finally, transient operation of the TEG is

investigated to understand the response of TEGs subjected to a change in the background heat flux.

2 Computational Methodology

This section outlines the computational methodology used in developing model for the package and embedded TEGs. The model for TEGs embedded within an electronic package is developed using the commercial computational fluid dynamics (CFD) package FLUENT and meshing software GAMBIT. The model solves Fourier's conduction equations for the electronic package and the TEG modules and provides temperature distributions for the entire system. The TEG modules are attached at the back side of the heat spreader. Each module has 49 p-n couple and has an area of $3\text{ mm} \times 3\text{ mm}$. The TE material is Bi_2Te_3 based superlattice which is $8\text{ }\mu\text{m}$ thick sandwiched between two $46\text{ }\mu\text{m}$ thick copper layers, resulting in a total TEG thickness of $100\text{ }\mu\text{m}$. The computational domain of the model includes the heat spreader, thermal interface material, chip, and TEGs. The properties of the TE and thermal interface material are obtained from the Ref. [11] and its supplementary material. The heat sink is modeled as a convective boundary condition at the top surface of the heat spreader with a convection coefficient, h , of $2050\text{ W/m}^2\text{-K}$. This value of convection coefficient is estimated from the previous computation by Gupta et al. [22] in order to match the numerical results of the packaged TEC with the experimental and numerical results presented in Ref. [11]. The detailed information about the heat sink geometry in Ref. [11] is not provided, but using the available information, the effective convection coefficient was estimated and results were within $1\text{--}2^\circ\text{C}$ of those presented in Ref. [11].

A schematic of the electronic package with the embedded TEGs can be seen in Fig. 1(a). The layout of the array of nine TEGs inside an electronic package is shown in Fig. 1(b) as needed for the simulations with multiple TEGs. Most of the simulations in the present work with a single TEG device correspond to TEG in the center position, which is location five in Fig. 1(b). The electrical and thermal contact resistances at the interface of the superlattice/metal layer ($10^{-11}\text{ }\Omega\text{ m}^2$; $10^{-6}\text{ m}^2\text{K/W}$) and the thermal contact resistance at the TEG/heat-spreader layer ($8 \times 10^{-6}\text{ m}^2\text{K/W}$) are

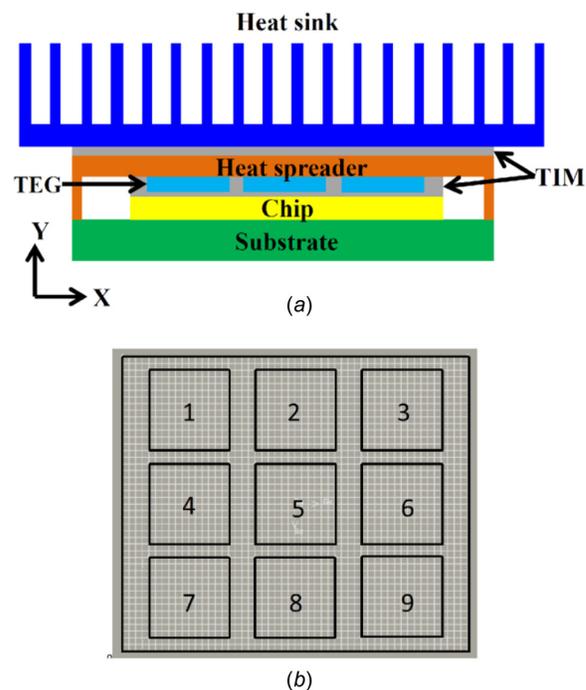


Fig. 1 (a) Schematic of the electronic package with embedded TEGs and (b) layout of the array of nine TEGs

taken from Ref. [11]. The geometry, thermoelectric properties, and contact resistances of packaged TEGs considered in the present work is similar to those of the TECs used in Refs. [22] and [23] and are also provided in Table 1. The cooling performance of these TECs has been validated against experimental results in our previous work [22].

3 Governing Equations

The governing differential equations for the thermal transport inside the electronic package is represented as

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \dot{Q} = \frac{\partial T}{\alpha \partial t} \quad (1.1)$$

where

$$\dot{Q} = \begin{cases} \frac{I^2}{A^2 \sigma k} & \text{inside TEC} \\ 0 & \text{elsewhere} \end{cases} \quad (1.2)$$

Here, T is temperature, α is thermal diffusivity, I is current, A is the area of an element, σ is electrical conductivity, and k is thermal conductivity.

A heat flux boundary condition is applied at the bottom of the chip, which can be expressed as

$$-k \frac{\partial T}{\partial y} = q'' \quad (1.3)$$

where $q'' = 42.7 \text{ W/cm}^2$ unless otherwise specified.

In addition, at the hot end of the TEG,

$$-kA \left. \frac{\partial T}{\partial y} \right|_{y=y_h^+} = \left[-kA \frac{\partial T}{\partial y} + SIT \right]_{y=y_h^-} + I^2 R_{\text{elec}} \quad (1.4)$$

Here, the y coordinate is directed from TEG to the heat spreader, and y_h^+ and y_h^- are locations just above and below the hot junction, respectively. S is the Seebeck coefficient and R_{elec} is the contact electrical resistance of the TEG. Also, at the cold end of the TEG

$$-kA \left. \frac{\partial T}{\partial y} \right|_{y=y_c^+} = \left[-kA \frac{\partial T}{\partial y} - SIT \right]_{y=y_c^-} + I^2 R_{\text{elec}} \quad (1.5)$$

where y_c^+ and y_c^- are locations just above and below the cold junction, respectively.

Finally, at the top surface of the heat spreader,

$$-k \frac{\partial T}{\partial y} = h(T - T_\infty) \quad (1.6)$$

where h is the convective heat transfer coefficient and T_∞ is the ambient air temperature, which is taken to be 300 K for all simulations.

Table 1 Dimensions and thermal conductivity of different components of the electronic package

| Component | Thermal conductivity (W/m-K) | Dimensions |
|----------------------------|------------------------------|--------------------------|
| Spreader | 400 | 30 mm × 1 mm × 30 mm |
| Thermal interface material | 1.75 | 11 mm × 0.125 mm × 13 mm |
| TEC-superlattice | 1.2 | 3 mm × 0.008 mm × 3 mm |
| Chip | 140 | 11 mm × 0.5 mm × 13 mm |

In addition to the material properties and boundary conditions of the package, thermoelectric power generation depends on the several factors: Seebeck coefficient, temperature difference between the hot and cold junctions of the TEG, and the resistances of the TEG and load. The equation for Seebeck voltage of TEG device can be given as

$$V = S(T_H - T_C) \quad (1.7)$$

where S is the Seebeck coefficient, T_H is the temperature of the hot junction, and T_C is the temperature of the cold junction. It is simple to determine the current through TEG once Seebeck voltage is estimated using the expression

$$I = \frac{V}{R} = \frac{S(T_H - T_C)}{R_L + R_{\text{TEG}}} \quad (1.8)$$

Here, R_L is the electrical resistance of load and R_{TEG} is the total electrical resistance of the TEG device (including contact resistances). The amount of useful work, W_U , is the power dissipated through the load resistance and can be evaluated by

$$W_U = I^2 R_L = \left[\frac{S(T_H - T_C)}{R_L + R_{\text{TEG}}} \right]^2 R_L \quad (1.9)$$

A current flows through the thermoelectric device when it is connected to external load which in turn reduce the temperature of the hot junction due to Peltier effects. Therefore, the Peltier effect must also be taken into account. Peltier cooling of the TEG device is incorporated by adding heat (αSIT_c) at the cold junction and subtracting heat (αSIT_h) from the hot junction of the TEG, where T_h and T_c are the temperatures of the hot and cold junctions, respectively. The value of S is considered to be $300 \mu\text{V/K}$ which is based on the experimental measurements in Ref. [11]. The heat generation due to the electrical resistance of the TEG device and the electrical resistances at contact is considered by adding an $I^2 R$ term at the corresponding volumes and layers. The thermal contact resistances were considered by adding appropriate thermal resistances at the interfaces.

The simulations are performed using the finite volume method based commercial solver FLUENT. 200 K cells are considered for the simulations; grid independence tests verify that these cells are sufficient for further simulations.

4 Power Generation Using Single TEG

This section studies the power generated by a single 3 mm × 3 mm TEG located at position five in Fig. 1(b) as a function of the load resistance. The current flow, voltage, and temperature across the TEG is investigated to understand the response of TEG embedded inside a micro-electronic package for a uniform background heat flux of 100 W/cm^2 at the bottom of chip.

4.1 Load Resistance. TEGs produce a Seebeck voltage under an applied thermal gradient which can be used to power an electrical device or circuit. The electronic circuits can be very complex, but for the simplicity of analysis we consider only a single load resistance connected in series with the TEG. Figure 2(a) shows the current flow and voltage across TEG as a function of the load resistance ($\sim 0-1 \Omega$). Figure 2(b) shows the temperature difference between the hot and cold junctions as a function of the load resistance. The electrical resistance of the TEG is 0.114Ω including both bulk material resistance and electrical contact resistance. As the load resistance increases, the Seebeck voltage and the temperature difference across TEG increases, but the current decreases. The increasing load resistance lead to decreasing current flow as expected from the relation in Eq. (1.9). Lower currents provide less Peltier cooling at hot side of TEG which increases the temperature difference and the Seebeck voltage as observed in Fig. 2.

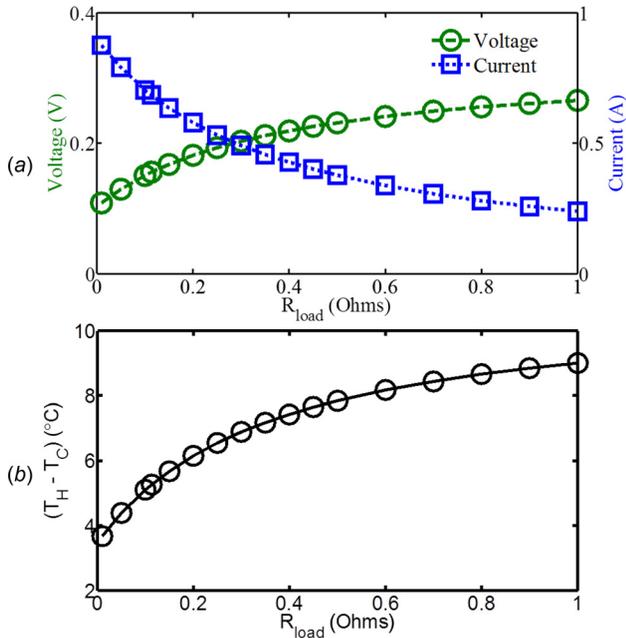


Fig. 2 (a) Voltage and current as a function of load resistance and (b) temperature difference between hot and cold junctions as a function of load resistance, for single TEG located at position five in Fig. 1(b)

The CRC handbook of thermoelectrics states that the maximum power transfer is obtained when the load resistance is equal to the TE device resistance [24]. In the present study, the maximum power transfer did not occur when the load resistance is equal to the TEG resistance. The total power and useful power as functions of load resistance are shown in Fig. 3. The total power is the addition of the power dissipated across the TEG and load as opposed to the useful power which is defined as the power dissipated across the load. The total power reaches its maximum value of 105 mW when the load resistance is equal to the device resistance ($\sim 0.114 \Omega$), but the useful power doesn't reach its maximum until 0.35Ω . The maximum useful power is 72.91 mW at this resistance. The reason the maximum useful power occurs at a different resistance is the dependence of Seebeck voltage on the temperature gradient across TEG which is in turn dependent on Joule heating and Peltier cooling. Maximum useful power transfer will occur when the load resistance equals the device resistance only for the systems that have fixed temperatures across TEG. In the present analysis, the final temperature drop across TEG is itself dependent on the current flow due to the Peltier cooling effect and self-consistent solution is necessary to estimate the current flow, voltage, and temperature across TEG. This is reflected in the

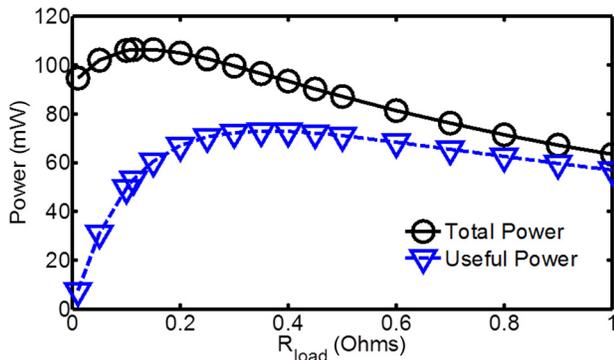


Fig. 3 Total power and useful power (in milliwatts) as a function of load resistance for single TEG at position five

deviation of maximum useful power from the point when load resistance is equal to TEG resistance. Similar trends were reported by Solbrekken et al. in their work but TEGs were attached outside of an electronic package [7].

In order to further understand the deviation of maximum useful power discussed above, we perform simulations where Peltier effect is not considered. Figures 4(a) and 4(b) show estimated current, voltage and power with no Peltier effects which is effectively keeping the voltage constant as the load resistance is changed. The maximum useful power is 234.56 mW when the load resistance is equal to the device resistance of 0.114Ω . This is consistent with the expected resistance for maximum power transfer. The change in the results of Figs. 2 and 3 compared to the Fig. 4 is only due to the inclusion of Peltier effects, which affect the temperature difference across the two junctions and hence change the Seebeck voltage. Therefore, the reason why the results in Fig. 3 differ from those expected for maximum power transfer is that the Peltier effects change the temperature gradient and voltage when load resistance is varied.

4.2 Background Heat Flux. TEGs can be used in conjunction with electronic packages for energy harvesting from waste heat. Heat dissipation varies in a wide range for electronic chips and significantly affects many design choices from the chip level up to the package level design and even further to server and building designs. This section investigates the effect of variation in the chip's background heat flux on TEG performance.

The steady-state operation of the single TEG is investigated with background heat fluxes ranging from 10 W/cm^2 to 100 W/cm^2 . The load resistance is set at 0.35Ω as this resistance is shown to provide the maximum useful power generation in the previous section. The Seebeck voltage and current as a function of background heat flux are plotted in Fig. 5(a). The voltage and current increase almost linearly with increasing background heat flux. The load resistance is kept constant in these simulations, so voltage and current are proportional to each other. The useful power generated at various background heat fluxes is shown in Fig. 5(b). As can be seen in this figure, the useful power increases in a parabolic form, which is expected since the current increases almost linearly and power is proportional to current-squared. At 100 W/cm^2 , the TEG generates 72.91 mW of useful power compared to 0.90 mW at

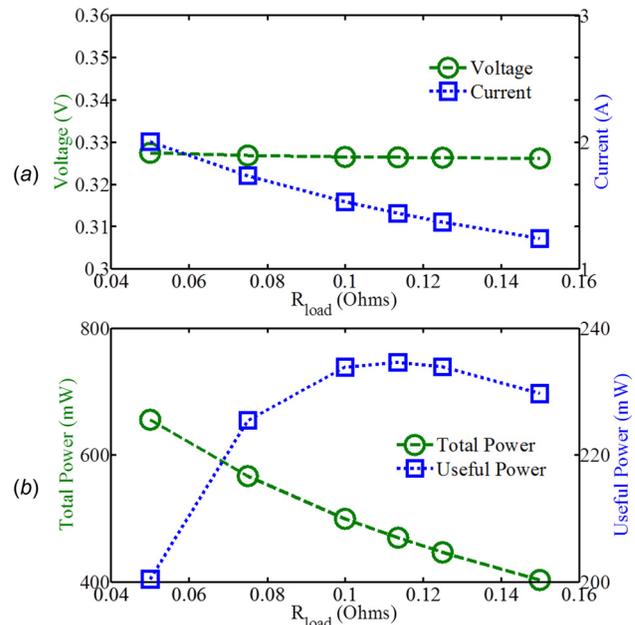


Fig. 4 (a) Voltage and current and (b) total power and useful power as a function of load resistance for single TEG at position five without considering Peltier effects

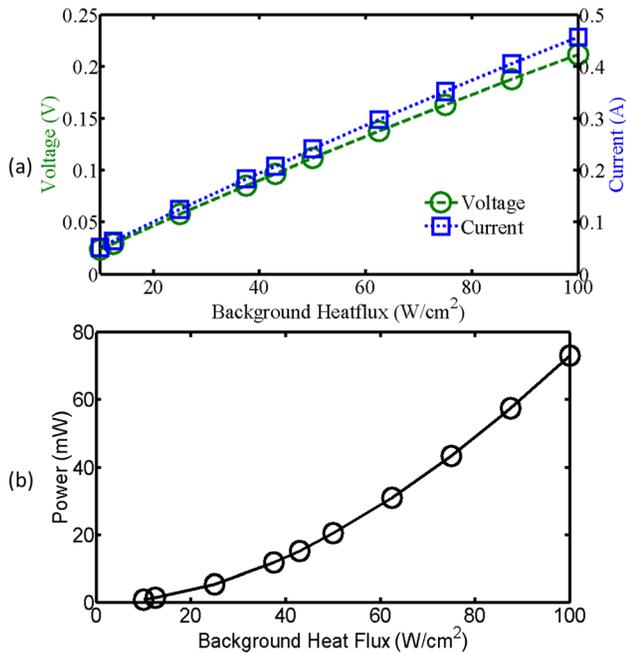


Fig. 5 (a) Voltage and current and (b) useful power as a function of background heat flux for single TEG at position five

10 W/cm². This parabolic increase in useful power with background heat flux shows the increased utility of TEGs as power densities on chip is kept on increasing from one generation to another generation.

Conversion efficiency is the indicator of the power generation efficiency of TEGs. The conversion efficiency of TEGs is indicator of the percentage of waste heat harvested into usable power and is defined as the amount of useful power divided by the heat flow through the hot junction. Figure 6 shows the conversion efficiency of the TEG as background heat flux increases. The conversion efficiency is observed to be almost linearly increasing with heat flux, e.g., conversion efficiency is 0.06% for 10 W/cm² and increases to 0.47% for 100 W/cm².

4.3 Proximity of TEG to Chip. The degree of cooling by a TEC can be enhanced by moving the device closer to the heat source [25]. However, the modification in the performance of embedded TEGs as a function of proximity to chip is not studied yet. In this section, we vary the TEG's proximity to the chip to investigate whether there are similar increases in the TEG performance. The TEG is moved from 48 μm to 3 μm in order to test the chip proximity's effect on TEG performance. Figure 7(a) shows the voltage and current as a function of proximity to chip. Figure 7(b) shows the resulting useful power obtained at a load resistance of

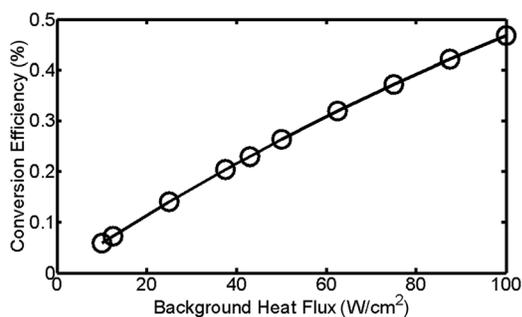


Fig. 6 Conversion efficiency of single TEG at position five as a function of background heat flux

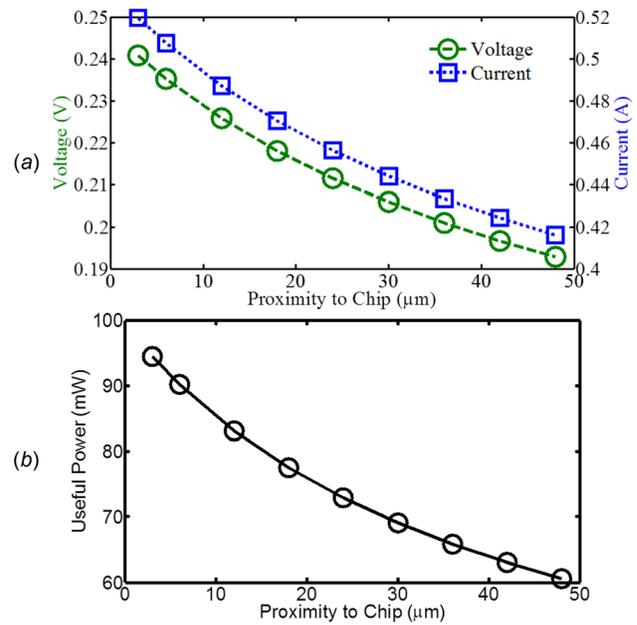


Fig. 7 (a) Voltage and current and (b) useful power as a function of TEG's proximity to chip for single TEG at position five

0.35 Ω. The voltage, current, and useful power all degrade as the device is moved away from the heat source or chip. This is due to a decrease in temperature difference between the hot and cold junctions as the device is moved away from the chip. Figure 8 shows the conversion efficiency as a function of proximity to chip. The conversion efficiency behaves similar to the useful power which is expected as the device is still the lowest resistance path for heat flow from chip to spreader and the heat flux through the device will not change drastically as it is moved further away from the chip. Section 5 investigates the use of multiple TEGs inside the package to harvest energy from chip waste heat.

5 Array of TEGs on Chip

The discussion in Sec. 4 is based on the simulation of single packaged TEG. This section will investigate the coupling effects of multiple TEGs on chip and how this coupling affects the total useful power. It is expected that adding more TEGs will provide additional power as they are capable of harvesting more waste heat from the chip. We investigate five different cases: (1) TEG 5 only; (2) TEGs 3, 5, and 7; (3) TEGs 1, 3, 5, 7, and 9; (4) All TEGs except 2 and 8; and (5) All TEGs 1–9. Here the location of TEGs corresponds to the setup depicted in Fig. 1. Figure 9 shows the total useful power generated by all TEGs present on the chip and the average useful power per TEG. The total useful power continues to increase as additional TEGs are added, but it is interesting to note that it is not a linear increase. Total useful power

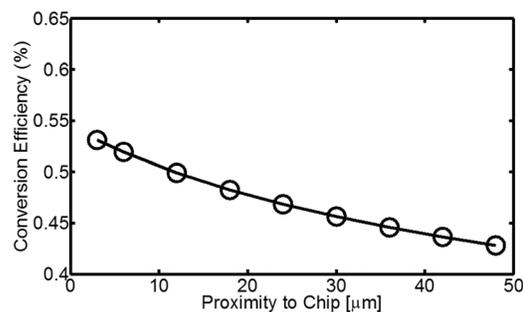


Fig. 8 Conversion efficiency of single TEG at position five as a function of TEG's proximity to chip

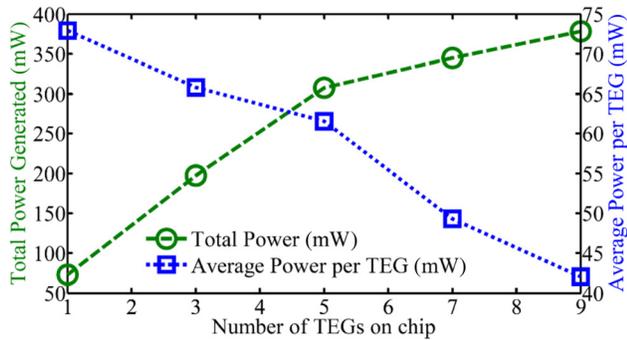


Fig. 9 Total useful power and average useful power per TEG in milliwatts for five setups with varying number of TEGs on chip: (1) TEG 5 only; (2) TEGs 3, 5, and 7; (3) TEGs 1, 3, 5, 7, and 9; (4) all TEGs except 2 and 8; (5) all TEGs 1–9. Numbering of TEGs corresponds to setup shown in Fig. 1.

increases in an approximately linear trend from one TEG to five TEGs on the chip, but this trend changes drastically for seven and nine TEGs. One TEG has a total useful power of 72.9 mW, five TEGs has 307.7 mW, and nine TEGs has 378.4 mW. Addition of four TEGs from case 1 to case 3 yields additional useful power of 234.8 mW but another four TEGs from case 3 to case 5 only yields additional useful power of 70.7 mW. This decrease in the additional power that each additional TEG provides is due to the crowding of the TEGs on chip. In cases 1–3, TEGs are well spread out at the center and corners of the chip. Cases 4 and 5, however, add TEGs on the sides in between the existing TEGs and end up degrading the performance of the TEGs already present on chip. Overall the total useful power still increases, but the gains from additional TEGs begin to diminish. The average useful power provided per TEG degrades from 72.9 mW per TEG for case 1 to 42.0 mW per TEG for case 5.

The conversion efficiency of the center TEG and the average conversion efficiency of all TEGs present on chip are shown in Fig. 10 for cases 1–5. The efficiency for case 1 with only the center TEG is approximately 0.47%. This is the highest efficiency per TEG out of all cases considered. The conversion efficiency of the center TEG at location five degrades drastically as more TEGs are added on the chip. The efficiency of center TEG decreases from 0.47% to 0.32% from case 1 of single TEG to case 5 of nine TEGs on the chip. Additional TEGs on chip reduces the heat flux through the center TEG as it is no longer the sole low resistance path, and this decreases the temperature difference between the hot and cold junctions significantly. The average conversion efficiency of all TEGs present on the chip is consistently higher than the efficiency of just the center TEG alone. This is due to the higher efficiency of the TEGs located at the corners, which help in raising the average efficiency of TEGs. The average conversion efficiency reduces from 0.47% to 0.36% from case 1 to case 5.

The results in this section show that additional TEGs on chip will always provide additional power generation, but TEG

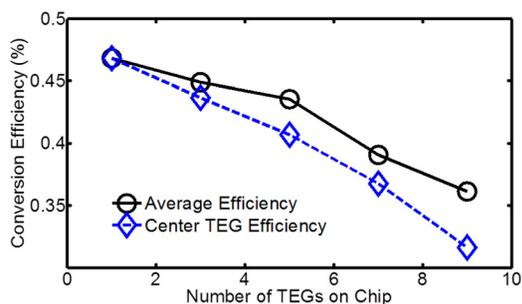


Fig. 10 Average conversion efficiency of all TEGs and of center TEG only for the five setups outlined in Fig. 9

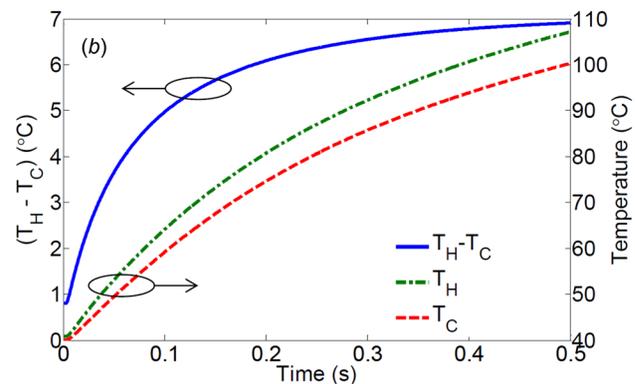
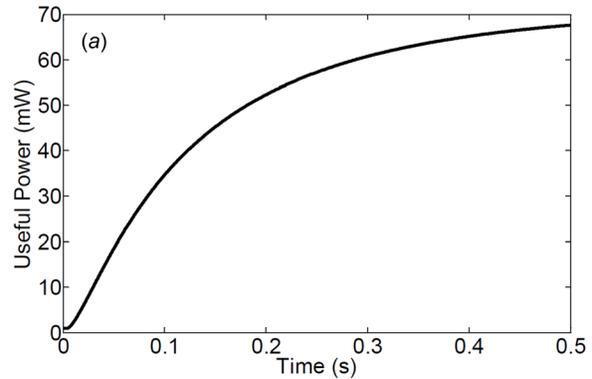


Fig. 11 Transient (a) useful power response and (b) hot (T_H) and cold (T_C) junction temperatures (right y-axis) and temperature difference ($T_H - T_C$) (left y-axis) of TEG when background heatflux changes from 10 W/cm^2 to 100 W/cm^2

conversion efficiency degrades as more TEGs are added on chip. Therefore, important design decisions need to be taken while designing a chip with embedded TEGs as there is an optimal number of TEGs for a desired total power.

6 Transient Response

In this section, we study the transient response of TEGs subjected to change in the background heat flux. Figure 11(a) shows the useful power of a TEG as the background heat flux is changed from 10 W/cm^2 to 100 W/cm^2 . We observe a small lag between the heat flux change and the initial response of the TEG due to the time needed in any significant change in temperature across the TEG. As soon as the temperature difference across the TEG start increasing, the useful power also begins to increase and finally approaches the steady-state useful power generation (72.9 mW) for 100 W/cm^2 . The temperatures of the hot and cold junctions of the TEG can be seen in Fig. 11(b). The difference in temperatures follow the same trend as the useful power, i.e., it increases with time and approaches to the steady-state solution for 100 W/cm^2 . A TEG is a passive device, so there are no extra benefits in power generation in transient operation due to the dynamic change in chip heat flux. The most useful aspect of the present transient simulations would be to make sure that the current or voltage across load components does not exceed their given thresholds. The slow response time of the TEG to the changes of the background heat flux appears to prevent any sudden spikes in current or voltage and there is no harmful impact on the external loads.

7 Conclusion

This work investigates the power generation by a single TEG and an array of TEGs embedded within a chip package. The optimum load resistance for maximum power generation is found to

be 0.35 Ω , which deviates from the initial expectations of the load resistance to be equal to the device resistance (0.11 Ω). This discrepancy is found to be due to the TEG's performance dependence on the temperature difference between the hot and cold junctions, which changes with the current and resulting Peltier effect. Increasing background heat flux increases temperature difference across the TEG and results in higher power generation. Temperature difference across TEG also increases when it is moved closer to the chip resulting in increase in useful power generation. The total useful power increases from 72.9 mW to 378.4 mW as the number of TEGs in the package is increased from one to nine. The negative aspect of having more TEGs on chip is the average power generated per TEG decreases from 72.9 mW per TEG for a single TEG to 42.0 mW per TEG for nine TEGs. Transient behavior of TEGs in response to increasing heat flux shows no advantage in power generation. The net power generation from TEGs will continue to improve as better thermoelectric materials will be discovered. There are interesting design choices to be made when embedding TEGs in chip. In future work, one of the important steps to consider is to address the specifics of how the power generated by TEGs can be utilized on chip and which portions of the chip will benefit most from this technology.

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Nomenclature

I = current (A)
 R_L = load resistance (W)
 R_{TEG} = device resistance (W)
 S = Seebeck coefficient (V/K)
 t = time (s)
 T = temperature ($^{\circ}$ C)
 V = voltage (V)

References

- [1] Bell, L. E., 2008, "Cooling, Heating, Generating Power, and Recovering Waste Heat With Thermoelectric Systems," *Science*, **321**(5895), pp. 1457–1461.
- [2] DiSalvo, F. J., 1999, "Thermoelectric Cooling and Power Generation," *Science*, **285**(5428), pp. 703–706.
- [3] Thacher, E. F., Helenbrook, B. T., Karri, M. A., and Richter, C. J., 2007, "Testing of an Automobile Exhaust Thermoelectric Generator in a Light Truck," *Proc. Inst. Mech. Eng., Part D*, **221**(D1), pp. 95–107.
- [4] Wang, Z. Y., Leonov, V., Fiorini, P., and Van Hoof, C., 2009, "Realization of a Wearable Miniaturized Thermoelectric Generator for Human Body Applications," *Sens. Actuators, A*, **156**(1), pp. 95–102.
- [5] Zhao, L.-D., Lo, S.-H., Zhang, Y., Sun, H., Tan, G., Uher, C., Wolverton, C., Dravid, V. P., and Kanatzidis, M. G., 2014, "Ultralow Thermal Conductivity and High Thermoelectric Figure of Merit in SnSe Crystals," *Nature*, **508**(7496), pp. 373–377.
- [6] Crane, D. T., LaGrandeur, J. W., Harris, F., and Bell, L. E., 2009, "Performance Results of a High-Power-Density Thermoelectric Generator: Beyond the Couple," *J. Electron. Mater.*, **38**(7), pp. 1375–1381.

- [7] Solbrekken, G. L., Yazawa, K., and Bar-Cohen, A., 2008, "Heat Driven Cooling of Portable Electronics Using Thermoelectric Technology," *IEEE Trans. Adv. Packag.*, **31**(2), pp. 429–437.
- [8] Xie, G., Chen, Z., Sunden, B., and Zhang, W., 2012, "Numerical Predictions of the Flow and Thermal Performance of Water-Cooled Single-Layer and Double-Layer Wavy Microchannel Heat Sinks," *Numer. Heat Transfer, Part A*, **63**(3), pp. 201–225.
- [9] Xie, G., Liu, J., Zhang, W., and Sunden, B., 2012, "Analysis of Flow and Thermal Performance of a Water-Cooled Transversal Wavy Microchannel Heat Sink for Chip Cooling," *ASME J. Electron. Packag.*, **134**(4), p. 041010.
- [10] Xie, G., Liu, J., Liu, Y., Sunden, B., and Zhang, W., 2013, "Comparative Study of Thermal Performance of Longitudinal and Transversal-Wavy Microchannel Heat Sinks for Electronic Cooling," *ASME J. Electron. Packag.*, **135**(2), p. 021008.
- [11] Chowdhury, I., Prasher, R., Lofgreen, K., Chrysler, G., Narasimhan, S., Mahajan, R., Koester, D., Alley, R., and Venkatasubramanian, R., 2009, "On-Chip Cooling by Superlattice-Based Thin-Film Thermoelectrics," *Nat. Nanotechnol.*, **4**(4), pp. 235–238.
- [12] Venkatasubramanian, R., Siivola, E., Colpitts, T., and O'Quinn, B., 2001, "Thin-Film Thermoelectric Devices With High Room-Temperature Figures of Merit," *Nature*, **413**(6856), pp. 597–602.
- [13] Venkatasubramanian, R., Watkins, C., Stokes, D., Posthill, J., and Caylor, C., 2007, "Energy Harvesting for Electronics With Thermoelectric Devices Using Nanoscale Materials," IEEE International Electron Devices Meeting (IEDM 2007), Washington, DC, December 10–12, pp. 367–370.
- [14] Strasser, M., Aigner, R., Lauterbach, C., Sturm, T. F., Franosh, M., and Wachutka, G., 2003, "Micromachined CMOS Thermoelectric Generators as On-Chip Power Supply," 12th International Conference on Transducers, Solid-State Sensors, Actuators and Microsystems, Boston, MA, June 8–12, pp. 45–48.
- [15] Li, Y., Buddharaju, K., Singh, N., Lo, G. Q., and Lee, S. J., 2011, "Chip-Level Thermoelectric Power Generators Based on High-Density Silicon Nanowire Array Prepared With Top-Down CMOS Technology," *IEEE Electron Device Lett.*, **32**(5), pp. 674–676.
- [16] Min, C., Rosendahl, L. A., Condra, T. J., and Pedersen, J. K., 2009, "Numerical Modeling of Thermoelectric Generators With Varying Material Properties in a Circuit Simulator," *IEEE Trans. Energy Convers.*, **24**(1), pp. 112–124.
- [17] Xiao, H., Gou, X. L., and Yang, C., 2008, "Simulation Analysis on Thermoelectric Generator System Performance," 7th International Conference on System Simulation and Scientific Computing (ICSC 2008), Beijing, China, October 10–12, pp. 1183–1187.
- [18] Chen, M., Rosendahl, L. A., and Condra, T., 2011, "A Three-Dimensional Numerical Model of Thermoelectric Generators in Fluid Power Systems," *Int. J. Heat Mass Transfer*, **54**(1–3), pp. 345–355.
- [19] Crane, D. T., Kossakovski, D., and Bell, L. E., 2009, "Modeling the Building Blocks of a 10% Efficient Segmented Thermoelectric Power Generator," *J. Electron. Mater.*, **38**(7), pp. 1382–1386.
- [20] Gould, C. A., Shamma, N. Y. A., Grainger, S., and Taylor, I., 2011, "Thermoelectric Cooling of Microelectronic Circuits and Waste Heat Electrical Power Generation in a Desktop Personal Computer," *Mater. Sci. Eng., B*, **176**(4), pp. 316–325.
- [21] Snyder, G. J., and Ursell, T. S., 2003, "Thermoelectric Efficiency and Compatibility," *Phys. Rev. Lett.*, **91**(14), p. 148301.
- [22] Gupta, M. P., Sayer, M. H., Mukhopadhyay, S., and Kumar, S., 2011, "Ultrathin Thermoelectric Devices for On-Chip Peltier Cooling," *IEEE Trans. Compon., Packag. Manuf. Technol.*, **1**(9), pp. 1395–1405.
- [23] Sullivan, O., Gupta, M. P., Mukhopadhyay, S., and Kumar, S., 2012, "Array of Thermoelectric Coolers for On-Chip Thermal Management," *ASME J. Electron. Packag.*, **134**(2), p. 021005.
- [24] Rowe, D. M., 1995, *CRC Handbook of Thermoelectrics*, Taylor & Francis, New York.
- [25] Sullivan, O., Alexandrov, B., Mukhopadhyay, S., and Kumar, S., 2012, "Compact Model of Thermoelectric Coolers on a Micro-Electronic Chip," ASME Paper No. IMECE2011-64881.