# A Numerical Study on Comparing the Active and Passive Cooling of AlGaN/GaN HEMTs

Xiuping Chen, Fatma Nazli Donmezer, Satish Kumar, and Samuel Graham

***Abstract*— In this paper, the power density capability of AlGaN/GaN high-electron mobility transistors (HEMTs) made on Si, SiC, and diamond substrates were compared with devices on Si and SiC with integrated microchannel cooling. A device temperature limit of 200 °C was used to define the power density. The numerical model accounts for heat transfer from channel of the AlGaN/GaN HEMTs to the heat sink, fluid flow rates, pressure drop, and pumping power required for liquid cooling. The diamond substrate was shown to be superior in reducing the junction temperatures in conventional passive cooling methods employing high thermal conductivity substrates. However, single-phase liquid cooling with microchannels integrated into a SiC substrate showed that it is possible to operate the devices at power densities higher than that on 200-$\mu$m-thick diamond substrates, considering a maximum operational temperature of 200 °C. Microchannels integrated into the Si substrate also showed a slight increase in the power density compared with passively cooled devices on SiC. Overall, this methodology shows a promising alternative to expensive high thermal conductivity substrates for cooling AlGaN/GaN HEMTs.**

***Index Terms*— Gallium nitride (GaN), high-electron mobility transistors (HEMTs), microchannel cooling, semiconductor device substrates.**

## I. Introduction

AlGaN/GaN high-electron mobility transistors (HEMTs) have been widely used for high power and high-frequency RF communications due to their fast switching and large current handling capabilities. The reliability of such devices is strongly affected by the junction temperature where the highest magnitude occurs in a local region on the drain side edge of the gate called the hotspot. Thus, thermal management of these devices remains as a major concern in the design and reliability of systems employing AlGaN/GaN HEMTs. Due to the high-power densities induced in these devices locally near the drain side edge of the gate, it is clear that moving thermal management solutions closer to the heat generation region is critical in order to reduce the overall junction temperature of the device. A number of solutions have been proposed to reduce the junction temperatures in AlGaN/GaN HEMTs [1]–[4]. These solutions include the use of high thermal conductivity substrates such as diamond [5] and microchannel cooling to effectively remove thermal energy from the device [4].

The majority of AlGaN/GaN HEMTs are grown on SiC substrates due to its high thermal conductivity (∼400 W/mK), which is ∼2.5 times that of GaN. However, the use of SiC is not always sufficient for devices operating at high-power densities. As an alternative to SiC, diamond substrates have a much higher thermal conductivity being a factor of 3 and 4 higher than SiC and are of interest for thermal management in AlGaN/GaN HEMTs [6]. Alternatively, for some applications, it is highly desirable to fabricate devices on Si substrates due to its lower cost and the availability of large diameter substrates for process scaling. However, Si has a much lower thermal conductivity than SiC, being on the order of 145 W/mK at room temperature. Thus, challenges exist in trying to make high-power density devices on Si substrates that will require new thermal management approaches.

As an alternative to using high thermal conductivity substrates, liquid cooling methods, such as microchannel liquid cooling, are used to reduce the temperatures in high-power electronics [7], [8]. Previous studies on the use of microchannel cooling on AlGaN/GaN HEMTs were focused on building microchannels in the heat sink attached to the substrate layer [9]. However, more efficient cooling may be achieved by placing microchannels directly under the substrate to effectively remove the thermal energy through convection versus conduction when high thermal conductivity substrates are used. While this method has been proposed for Si devices, its integration in AlGaN/GaN HEMTs has not been implemented as of yet.

In this paper, we report a comparison of the use of passive cooling methods via conduction through the device substrate and active cooling methods on the thermal performance of AlGaN/GaN HEMTs. The method employs a computational fluid dynamics model to capture the fluid flow, pressure drop, and thermal distribution in the packaged devices. A comparison is made between the passive and active approaches to determine where active cooling with microchannels integrated in the substrate can extend the performance range of devices and where passive cooling remains most effective.

## II. System Layout and Device Geometry

In this paper, the junction temperatures in 30-finger AlGaN/GaN HEMTs on Si, SiC, and diamond substrates were investigated. The die is 2-mm long and 1-mm wide. It is

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TABLE I
THERMAL CONDUCTIVITY [10]–[12] FOR ALL SUBSTRATES AND TBR [3]–[13] BETWEEN THE SUBSTRATE AND GaN LAYER. TBR FOR GaN-ON-DIAMOND DEVICES [3] IS ALSO SHOWN. * IS IN PLANE AND ** IS OUT OF PLANE

| Substrate | Thermal Conductivity [W/m-K] | Thermal Boundary Resistance [x $10^{-8}$ $W^{-1}m^2K$] |
|---|---|---|
| SiC | $387\times[\frac{T}{293}]^{-1.49}$ | 3.3 |
| Si | $148\times[\frac{T}{300}]^{-1.3}$ | 3.3 |
| Diamond | $0.003\times T^2-4.238\times T+2478$ * <br> $0.0024\times T^2-3.397\times T+1983$ ** | 3.6 |

TABLE II
THICKNESS AND THERMAL CONDUCTIVITY [10] OF THE MATERIALS USED IN SIMULATIONS

| Material | Thickness [μm] | Thermal Conductivity [W/m-K] |
|---|---|---|
| GaN | 2 | $150\times[\frac{T}{300}]^{-1.4}$ |
| AuSn/Solder | 50 | 57 |
| CuW | 640 | $204-0.0251\times T-0.0000762\times T^2$ |
| Epoxy | 50 | 2.5 |
| Cu | 5000 | 387 |

attached to a commercially available CuW microwave lead amplifier package with a 50-$\mu$m-thick AuSn solder layer. The package is mounted on a heat sink (a copper cold plate) using a 50-$\mu$m-thick thermal epoxy layer. The thermal properties of each material and thickness of each layer are listed in Tables I and II.

The thermal behaviors of the system under passive and microchannel liquid cooling were investigated, as discussed in Section III. In the passive cooling case, HEMT devices on Si, SiC, and diamond substrates with a different substrate thickness were analyzed. For microchannel liquid cooling, the microchannels were built into a separate substrate that was attached directly to the backside of the die. The microchannel cooled die was attached to the CuW package by a thin layer (50 $\mu$m) of AuSn solder. Gate-to-gate spacing of 30, 40, and 50 $\mu$m were analyzed in both passive and active microchannel cooling architectures.

## III. MODEL DEFINITION

In all the cases, thermal simulations were performed for the entire system, accounting for multiple length scales in one model. The transition layer between GaN and substrate was replaced by a thermal boundary resistance (TBR) in the thermal model. The Joule heating in each channel was approximated by a surface heat flux on top of the GaN layer with an area of 150-$\mu$m wide by 0.5-$\mu$m long, as shown in Fig. 1.

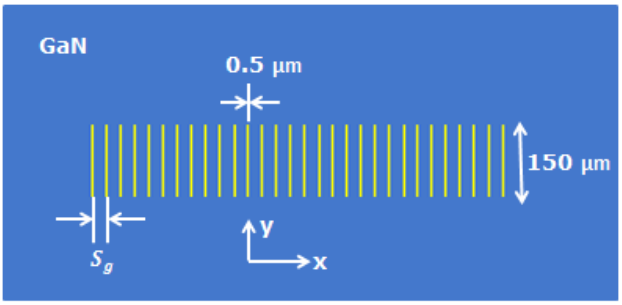


Fig. 1. Top view of a 3-D model with 30 identical heat flux areas on top of GaN layer. Dimensions of the heat flux areas are labeled. $S_g$ is gate-to-gate spacing. Yellow lines: heat flux area under each gate electrode.

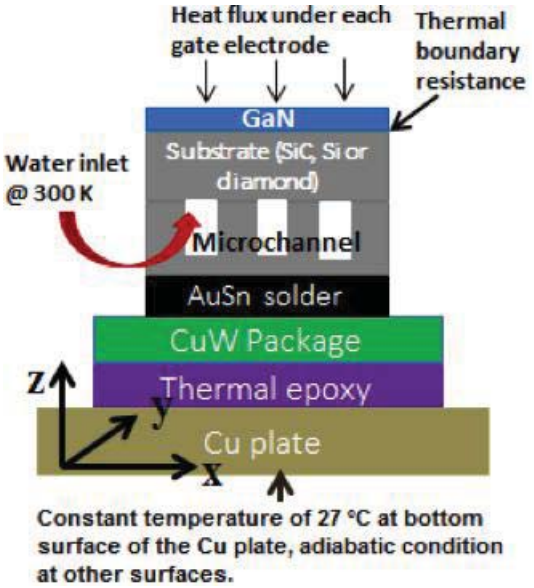


Fig. 2. Side view of a 3-D model for microchannel cooling with microchannels built on a Si or SiC (or diamond) wafer and attached to the Si or SiC (or diamond) substrate. A constant temperature of 27 °C is applied to the bottom of the Cu plate. Heat flux is applied on top of GaN layer, as shown in Fig. 1. Direction of fluid flow aligns with the width ($y$-direction in the fingers).

### A. Passive Cooling

A 3-D model was created for the passive cooling case. Depictions of the system modeled are shown in Figs. 1 and 2. In the case of passive cooling, microchannels are not present under the substrate. All surfaces, except the heat flux regions and bottom surface of the copper plate were set as adiabatic. The bottom surface of the copper plate was set to a constant temperature of 27 °C, which represents the center of the cold plate where the fluid is flowing. Due to the symmetric nature of the problem, only a quarter of the system was simulated. In this case, the effect of the substrate thickness on the peak temperature was investigated. The optimum thickness for each substrate material was found as a function of gate-to-gate spacings of 30, 40, and 50 $\mu$m. The optimal thickness was then used in microchannel liquid cooling in this paper.

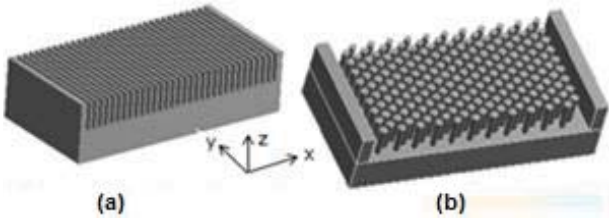


Fig. 3. Isometric views of linear fin and pin fin microchannel coolers. (a) Linear fin microchannel. (b) Pin fin microchannel.

### *B. Active Cooling Using Integrated Microchannels*

The microchannel liquid cooling model is shown in Fig. 2. Thermal-fluid simulations for the whole system were performed using ANSYS Fluent software. Due to the symmetric nature of the problem, only half of the system was modeled. Both GaN-on-Si and GaN-on-SiC with integrated microchannel coolers were analyzed with two different microchannel geometries (linear fin and pin fin). GaN-on-diamond was analyzed with pin fin microchannels only. For both configurations, the following assumptions were made. Water was used as the heat transfer fluid with temperature-independent properties except viscosity. The validation of this assumption was discussed in [14] and [15]. The fluid flow remained in laminar regime with an inlet temperature of 27 °C and remained single phase. A maximum pressure drop of 200 kPa was used as a pressure drop limit. The maximum power density was found by limiting the junction temperature to 200 °C. All surfaces except the heat flux areas, fluid-solid interface, and the bottom surface of the copper plate, were set as adiabatic boundary conditions. As with the passive cooling case, a constant temperature of 27 °C was applied to the bottom surface of the copper plate.

The first microchannel cooler considered contained a linear channel arrangement, as shown in Fig. 3(a). Practical dimensions for the cooler were taken from previous studies [16], where Si microchannels were successfully fabricated and used in experiments. The Si microchannels attached to the backside of the substrate had a height Hc of 250 $\mu$m and width $W_c$ of 35 $\mu$m. The wall thickness $W_t$ was 25 $\mu$m. There were 32 channels in total. The high aspect ratio of the SiC etching used here has been studied and shown to be feasible [17].

As an alternative to the linear microchannel array, a pin fin microchannel cooler was investigated, as shown in Fig. 3(b). Pin fin microchannels can increase the level of mixing in the fluid flow and thereby exhibit a higher convective heat transfer coefficient [18]–[21]. In this paper, staggered pin fins with different diameters, $D$, longitudinal spacing, $S_L$, and transverse spacing, $S_T$, were studied. Identical to the linear microchannel, the height of the pin fins were also 250 $\mu$m.

## IV. Results and Discussion

### *A. Passive Cooling Results*

First, the minimum substrate thickness needed to minimize the thermal resistance was determined for each material and gate-to-gate spacing for the AlGaN/GaN HEMTs. An analytical approach for the thermal resistance of passively cooled

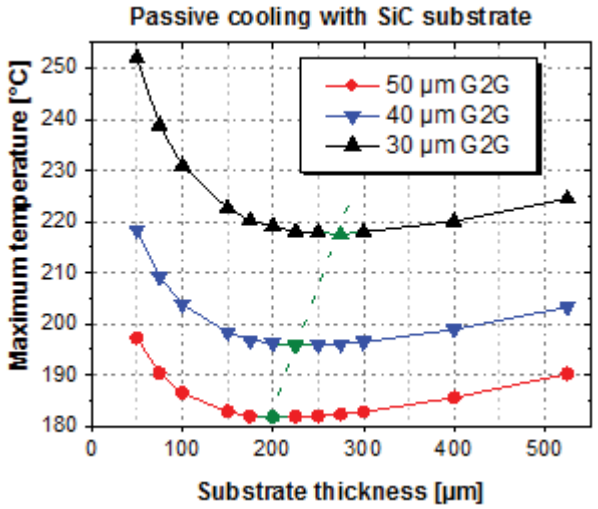


Fig. 4. Effect of SiC substrate thickness on maximum temperature for different gate-to-gate spacings with a power density of 4.1 W/mm in passive cooling.

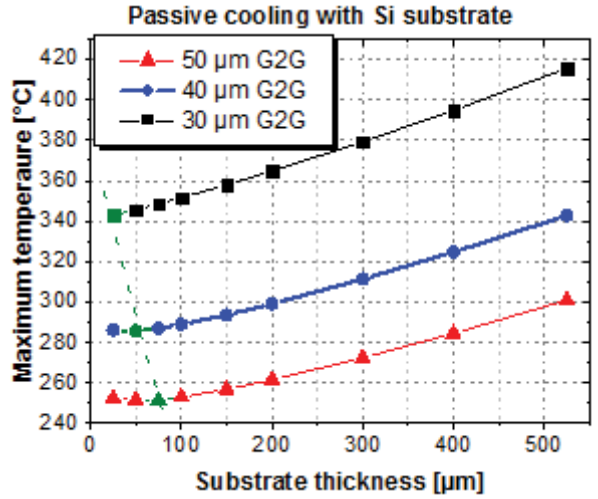


Fig. 5. Effect of SiC substrate thickness on maximum temperature for different gate-to-gate spacings with a power density of 4.1 W/mm in passive cooling.

GaN HEMTs with a backside constant temperature was given in [22], including Si and SiC substrates. An additional study in [23] investigated the impact of substrate thickness on the thermal resistance of AlGaN/GaN HEMTs that were backside mounted to either Cu or CuMo heat sinks. From [22] and [23], it was shown that the thermal resistance of a packaged AlGaN/GaN HEMT has a complex relationship to substrate thickness, gate length, gate width, and boundary conditions on the backside of the substrate. The results for our structure are shown in Figs. 4 and 5. For both the SiC and Si substrates, a reduction in the gate-to-gate spacing resulted in a higher maximum temperature for a fixed substrate thickness and linear power density as seen in [22]. For GaN-on-SiC, the minimum substrate thickness that resulted in the minimum device temperature increased from 200 to 275 $\mu$m for a decreasing gate-to-gate spacing of 50 to 30 $\mu$m, which follows the trend in [22]. GaN-on-Si has somewhat of a different trend as shown in Fig. 5. The minimum substrate thickness for

Si was observed to increase from 25 to 75 $\mu$m with increasing gate-to-gate spacing from 30 to 50 $\mu$m. The thicknesses for Si are much smaller than those for SiC. This is due to the fact that the Si has much lower thermal conductivity than SiC. While increasing the substrate thickness helps to decrease the spreading resistance in both SiC and Si substrates, the 1-D thermal resistance increases more rapidly in the Si than the SiC substrate. Therefore, the tradeoff in thickness for Si is much smaller than for the SiC substrate.

Based on the results shown in Figs. 4 and 5, a 200-$\mu$m-thick SiC substrate and 75-$\mu$m-thick Si substrate were used as a baseline passively cooled case for all gate-to-gate spacings. The results in Figs. 4 and 5 show that the junction temperature does not vary greatly with thickness near the minimum point, thus a single value can be used without much penalty for each substrate material. It should be noted that these values may not be the minimum values for the active cooling case. In [23], it was clearly shown that if the thermal conductivity of the layers underneath the die are large, then die thinning can be used to reduce thermal resistance. However, if the conductivity is small, then die thinning may result in an increase in thermal resistance due to the lack of heat spreading. Thus, while we have fixed the substrate thickness to be the same in both the passive and active cooling cases, additional work may be necessary to truly minimize the thermal resistance under the active cooling case. However, this will rely on the flow rate, which changes the convective heat transfer coefficient and thus, becomes a complex problem that cannot be optimized for all flow conditions.

### *B. Microchannel Cooling*

With a linear microchannel array, the power density increases nonlinearly as the volumetric flow rate increases for both GaN-on-SiC and GaN-on-Si, as shown in Fig. 6. At low flow rates (<50 ml/min), the power density is very sensitive to flow rate, but as flow rate increases the slope decreases. When the flow rate is low, the hydrodynamic entry length is short, and fluid flow becomes fully developed inside the microchannel. It was found that at a flow rate of ~70 ml/min, the entry length reaches 1000 $\mu$m, which is the length of the linear microchannel. Therefore, fully developed flow occurs inside the microchannel when the flow rate is <70 ml/min. In the fully developed region, the local Nusselt number becomes constant and thus the heat transfer coefficient becomes constant. At this point, increasing the flow rate will increase the entry length and decrease the fully developed region inside the microchannel. This explains the high sensitivity of power density to flow rate at low flow rates. When further increasing the velocity, the bulk fluid temperature rise decreases but at a decreasing rate. So, the junction temperature becomes less sensitive to the velocity. The Reynolds number was between 30.55 and 733.2 for linear microchannels and between 162.6 and 514.1 for pin fin microchannels. Therefore, the laminar flow model was valid for all simulations.

The power densities for GaN-on-SiC and GaN-on-Si with pin fin microchannels are shown in Fig. 7. All pin fin geometries are listed in Table III. Under the same pressure drop

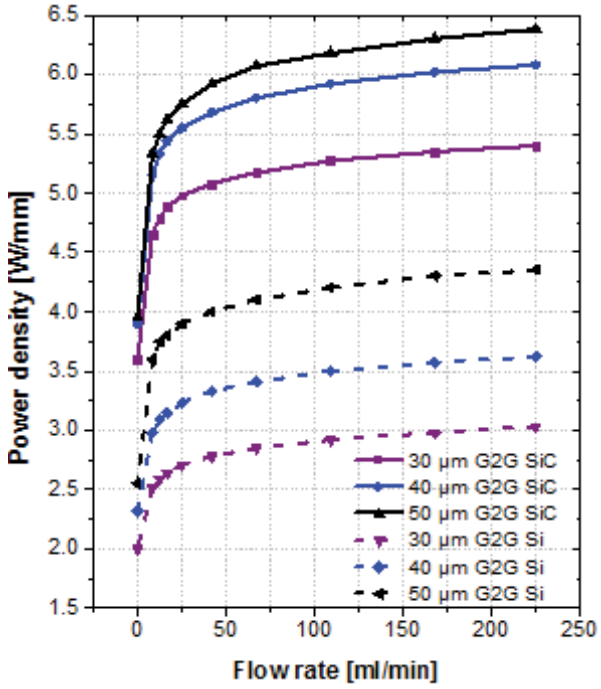


Fig. 6. Power density versus volumetric flow rate for linear fin microchannels. The power density is the maximum power density in the device to have a junction temperature no >200 °C.

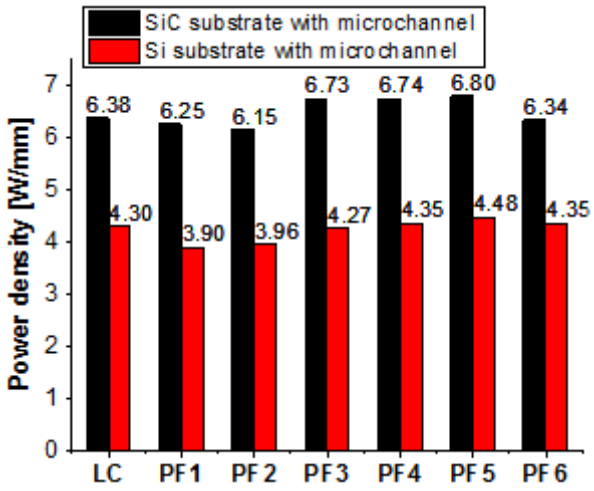


Fig. 7. Comparison of power density between different microchannel designs under the 200 °C maximum temperature and 200-kPa pressure drop conditions. *LC* is linear channel. PF is pin fin channel. 50-$\mu$m gate-to-gate spacing for all cases.

of 200 kPa and maximum junction temperature of 200 °C, pin fin 5 with a diameter of 50 $\mu$m, longitudinal spacing of 50 $\mu$m, and transverse spacing of 75 $\mu$m has the highest power densities—4.48 and 6.8 W/mm for GaN-on-Si and GaN-on-SiC, respectively. These power densities translate to 10.08 and 15.3 W/mm$^2$ on average. Although the performance of linear microchannels *LC* is close to the pin fin microchannel in terms of power density, the volumetric flow rate for the pin fin microchannels was only a quarter of that for the linear microchannels, resulting in a 75% reduction in pumping power while using pin fins.

TABLE III
PIN FIN DIAMETERS AND SPACINGS FOR PIN FIN MICROCHANNEL $S_L$ REPRESENTS LONGITUDINAL SPACING AND $S_T$ REPRESENTS TRANSVERSE SPACING

| Symbol | Diameter [μm] | $S_L$ [μm] | $S_T$ [μm] |
|---|---|---|---|
| PF1 | 50 | 100 | 100 |
| PF2 | 50 | 75 | 100 |
| PF3 | 50 | 50 | 100 |
| PF4 | 60 | 60 | 90 |
| PF5 | 50 | 50 | 75 |
| PF6 | 40 | 40 | 60 |

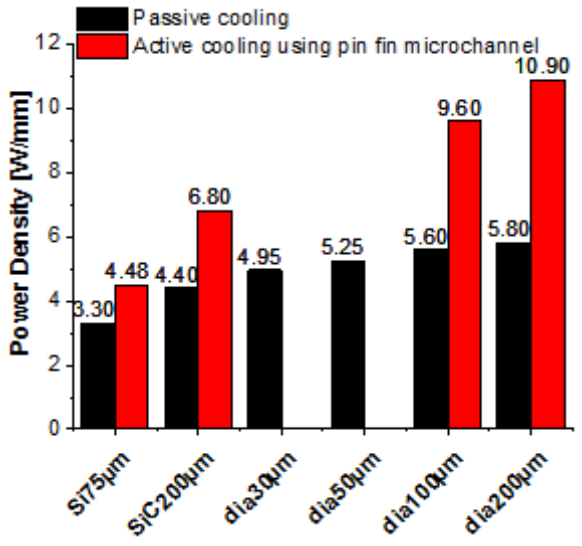


Fig. 8. Comparison of power density between passive cooling and active cooling with pin fin microchannel (PF5 geometry). All cases are under the 200 °C maximum temperature condition. Cases with microchannel cooling have 200-kPa pressure drop and 50-$\mu$m gate-to-gate spacing for all cases. dia200 $\mu$m is 200-$\mu$m diamond substrate.

Fig. 8 shows a comparison of the maximum power density that can be dissipated by the active and passive cooling approaches with different substrate materials. GaN-on-diamond with an embedded diamond microchannel for liquid cooling was also investigated for comparison, which represents the best that single-phase liquid cooling can provide. The data show that the active microchannel cooling in Si substrates is nearly the same as passive cooling in SiC substrates in terms of power density. However, embedding microchannels in SiC substrates has a great impact, dramatically outperforming 200-$\mu$m-thick passively cooled diamond substrates.

## V. CONCLUSION

The use of active cooling through the incorporation of embedded microchannels in AlGaN/GaN HEMTs is an alternative to using passive cooling methods involving high thermal conductivity substrates. It was found that the use of pin fin microchannel geometries provides additional benefits over that seen for linear microchannels, namely a reduction in the required pumping power for a similar maximum power density. While microchannels in SiC substrates show benefits when comparing devices to diamond substrates, the reliability of such microchannel pumped systems will need to be proven. Thus, passive cooling methods may still be preferred in some cases where reliability is paramount. The biggest benefit seen through this paper is the use of embedded channels in SiC. In comparing embedded channels in SiC and Si, devices on SiC can handle power densities that are 50% larger. Additional benefits may be seen if the substrate thickness is optimized for the targeted flowrate expected to be used in the device. Thus, single-phase liquid cooling embedded in these devices is attractive since it improves the power handling capabilities while leveraging the larger industrial base that has been developed in growing reliable AlGaN/GaN HEMTs on SiC substrates.

As the proposed microchannel cooling system has shown improvements in transistor-level power density, it has potential to improve the power density at the system level as well. However, several system level considerations which may impact the size of the system containing a microchannel pump and heat exchanger must be considered when implementing a microchannel cooling system versus passive technologies. In addition, improvements of TBR between GaN and high thermal conductivity substrates such as diamond [24] are expected to bring significant reduction in overall thermal resistance in passively cooled systems. This may also be important in any microchannel cooled systems where TBR is also high due to the nucleation of the GaN layer during epitaxial growth. The cost of implementing a micro-pump system, the required pumping power, the reliability of the pump, and so on are crucial parameters, which should be also estimated and compared with the cost of high thermal conductivity substrates.

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