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Thin dielectric-layer-enabled low-voltage operation of fully printed flexible carbon nanotube thin-film transistors

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Abstract

The quality of printable dielectric layer has become one of the major obstacles to achieving high-performance fully printed transistors. A thick dielectric layer will require high gate voltage to switch the transistors on and off, which will cause high power dissipation in printed devices. In response to this challenge, fully printed carbon nanotube (CNT)-based thin-film transistors (TFTs) have been fabricated on flexible membranes such as polyimide and liquid crystal polymer using aerosol jet printing. These devices can be operated at bias voltages below ± 10 V (drain/gate voltages around ± 6 V). This is much smaller than the previously reported values for fully printed CNT-TFTs because of using xdi-dcs (mixture of poly(vinylphenol)/poly (methylsilsesquioxane)) as the dielectric and using a single printing method. The lower voltage is a consequence of a thin dielectric layer ($\sim$300 nm) and good uniformity in the printed CNT network. The printed CNT-TFTs show on/off ratio $>10^5$, and mobility >5 cm^{2}V^{-1}s^{-1}. Layer-by-layer deposition of CNT allows highly uniform and dense network formation, and the optimization of the xdi-dcs concentration using natural butyl alcohol provides high-yield printing of a thin dielectric layer. Collectively, this work shows the potential of using fully printed CNT-TFTs in various flexible electronic applications such as wearable sensors, actuators, artificial skin, displays and wireless tags and antennas.

Supplementary material for this article is available online

Keywords: fully printed thin-film transistors, printed dielectric, xdi-dcs, carbon nanotube network, flexible electronics, aerosol jet printing

(Some figures may appear in colour only in the online journal)

1. Introduction

Printed electronics on flexible substrates has attracted significant attention in recent years because of the high potential in wearable and bendable devices [1]. Its applications include flexible displays [2], radio frequency identification (RFID) antennas/tags [3, 4], sensors [5, 6], artificial skin [7], etc. Among various printing techniques, aerosol jet printing (AJP) has been proven to be capable of printing microelectronic devices and relevant circuits at low cost, with repeatability, scalability and relatively high precision compared with other printing techniques [8, 9]. AJP has been utilized to deposit a

wide range of materials because it can handle ink viscosities in the range of 1–1000 Cp [10]. The superior electrical, mechanical and chemical properties of single-walled carbon nanotubes (CNTs) make them very promising as the channel material in thin-film transistors (TFTs) [11, 12]. As a 1D nanoscale material, CNT has exceptional high current carrying capacity [13, 14]. Extraordinary flexibility [15–17] and elasticity [18] can also be expected when CNT undergoes high strain and bending, which is also the key advantage of using CNT for flexible devices. Printed CNT-TFTs with improved carrier mobility, device stability, variability and dissipation power have significant potential for many applications [19–23].

In addition to the advances in printing techniques, the synthesis and processing of nanomaterials have brought fresh impetus to the development of printed flexible devices [24], but the tradeoff between cost and performance still limits their applications. Fully printed CNT-TFTs are crucial for low-cost fabrication because lithography steps and deposition techniques such as atomic layer deposition (ALD), typically used for gate-dielectric synthesis, will complicate the process and increase the cost at the same time. On the other hand, high performance is hard to achieve for fully printed CNT-TFTs. There are different causes, such as imperfections in the electrode patterns, contact quality at the interfaces, uniformity of the CNT network, thickness of the dielectric layer, etc [25]. Most of these causes need to be addressed properly, using, for example, nanoparticle silver (Ag) inks [26] for contacts, highly purified semiconducting CNT inks [27] for TFT-channel; and ion gels, barium titanate ($BaTiO_3$), xdi-dcs, etc, as dielectric inks [28–31]. Here, xdi-dcs is a blend of poly (vinylphenol)/poly(methylsilsesquioxane) (PVP/pMSSQ).

In previous studies, flexible CNT-TFTs were fabricated using different printing techniques, including inkjet printing (IJP) [19, 32, 33], AJP [8, 10, 34], screen printing [35], roll-to-roll gravure [5, 36, 37], as well as some combination of printing systems [36]. For fully printed CNT-TFTs, one of the primary obstacles to enabling low-voltage operation lies in printing a good quality gate-dielectric layer because of the lack of high-quality printable inks. One of the most straightforward solutions to address this is to use ALD for the dielectric deposition. Kim *et al* fabricated CNT-TFTs using a combination of IJP and ALD [33]. Electrodes, semiconductors and vias were realized by IJP, but Al_2O_3 was deposited using ALD as the dielectric layer, which resulted in ambipolar transistors and circuits with high operational stability. Like Kim, most of the previous work used nonprinting methods to pattern dielectrics or some other elements of TFTs during fabrication. Homenick *et al* demonstrated fully printed CNT-TFTs using an integrated roll-to-roll gravure/IJP system (not a single printing system) [36], which yielded good CNT network uniformity in fully printed TFTs on liquid crystal polymer (LCP) substrates. Cai *et al* also reported fully printed CNT-TFTs using a hybrid gate dielectric comprising PDMS and $BaTiO_3$ nanoparticles [30]. Cao *et al* pointed out the disadvantages of $BaTiO_3$/PMMA as the gate dielectric, which highly depends on the size, shape and spatial distribution of nanoparticles [31]. In their work, a thick

hydrophobic layer using xdi-dcs was printed as the gate dielectric ($\sim 2\,\mu$m, to avoid pinholes) of CNT-TFTs on Kapton substrate leading to negligible hysteresis. However, this thick dielectric layer severely limited their performance, and achieving thin printed dielectric without pinholes is still very challenging. Cao *et al* investigated methods to improve the electric contacts in fully printed CNT-TFTs by employing different printed contact materials and contact geometries [20]. Andrews *et al* introduced eutectic gallium−indium liquid metal contacts for printed CNT-TFTs to achieve stretchable transistors [24]. Cardenas *et al* fabricated CNT-TFTs using a low-temperature and entirely in-place AJP approach without removal of the substrate from the printer. Low contact resistance to semiconducting CNTs was achieved without the use of high-temperature baking steps [38]. However, the high threshold voltage in these TFTs highly limited their performance because the gate bias has to be as large as ± 40 V to fully switch on/off the transistors. Ion gel could be an alternative solution to address the specific problem of high threshold voltage [28, 29, 39], but ion-gel-based printed CNT-TFTs exhibit ambipolar performance with high leakage and static power consumption [31]. Also, ion-gel is fragile compared to other dielectric materials.

In this work, fully printed CNT-TFTs were fabricated on both Kapton and LCP substrates utilizing only AJP technique. For comparison, some other CNT-TFTs (non-fully printed) were also fabricated, whose dielectric was grown by ALD. The performance of fully printed devices was significantly improved by optimization of the printed xdi-dcs layer, which can be a superior gate-dielectric material for printed devices because it avoids the issues reported in the previous studies by other researchers when using BaTiO3/PMMA [30] (particle-like printing) and ion gel [40] (stability, environment sensitive). The CNT network was printed as the channel material of TFTs using a solution of single-walled CNTs in toluene, whose concentration was 0.01 mg ml^{-1}. More than 99% of the CNTs in the solution were semiconducting. A highly uniform CNT network film was achieved by performing a layer-by-layer deposition, which largely decreases the CNT bundling effect and provides an effective means of density control. Printing of single conductive layer of CNT network improved the on/off ratio of the fully printed devices. The printing of xdi-dcs thin film as the gate dielectric was realized by diluting and optimizing the ink with natural $\geqslant 99.5$% butyl alcohol in appropriate wt-%, and applying plasma treatment for better surface wetting. The fabricated CNT-TFTs showed very stable performance with on/off current ratio as high as $\sim 10^5$, mobility with average value of 4.9 cm^{2}V^{-1}s^{-1}, low hysteresis with average value of 0.6 V and good uniformity of the CNT network. More importantly, these TFTs can be operated under gate voltages below ± 10 V. For the first time, these CNT-TFTs are fabricated with a printed xdi-dcs layer as thin as ~ 300 nm, free of pinholes, leading to low-voltage operation. This work achieved the lowering of the operating voltage (± 6 V) for fully printed flexible devices using xdi-dcs as the dielectric based on a single printing method. This improvement is key for the application of CNT-TFT-based circuits in printed electronics
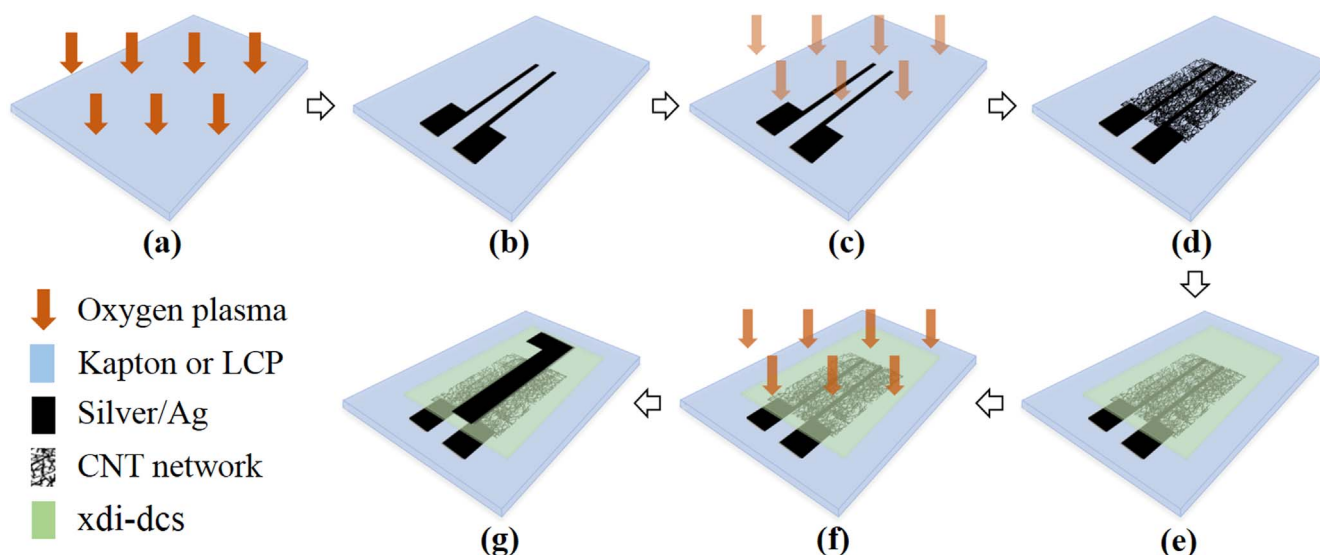
Figure 1. Schematic of the fabrication process of fully printed CNT-TFTs on flexible substrates using AJP. (a) Well prepared flexible substrate (either Kapton or LCP), which is cleaned with 3–5 min oxygen plasma before printing. (b) Ag printing to fabricate S/D electrodes. (c) 1 min oxygen plasma treatment before CNT printing for better wetting. (d) CNT network printing using a multiple layer-by-layer printing method. (e) Dielectric layer/xdi-dcs printing. (f) 2–3 min oxygen plasma treatment before Ag printing. (g) Ag printing as a top gate electrode. Fully printed CNT-TFT is fabricated following these steps. Note: Ag is cured at 150 °C for 15~25 min. Dielectric layer/xdi-dcs is cured at 140 °C for 20 min.

on flexible substrates because of the lower-voltage operation and lower power dissipation.

2. Experimental

The fabrication process of the fully printed CNT-TFTs is shown in figure 1. Kapton (DuPont, USA) with thickness of 127 μm ($\pm$10%) and LCP films (Rogers, USA) with thickness of 150–200 μm, were used as the flexible substrates. They were rinsed with acetone, isopropyl alcohol (IPA), and deionized (DI) water, successively, then blown dry by N_2 gun. Next, 5 min oxygen plasma (100 W) was applied for better surface preparation, which was followed by Ag printing (Ag ink: UTD Ag Conductive Silver Nanoinks, UT Dot) as source and drain (S/D) electrodes using the Optomec aerosol jet printing system AJ200. Then, Ag patterns were sintered at 150 °C for 15~25 min in an oven. Before CNT printing (CNT ink: IsoSol-S100® Polymer-Wrapped Nanotubes, NanoIntegris), 30 s oxygen plasma was applied to functionalize the surface, which could help achieve a uniformly distributed CNT network. A thorough cleaning of AJ200 was indispensable when changing from Ag to CNT ink (2~3 h ultrasonic, then acetone, IPA, DI water, and toluene rinse, successively). After CNT printing, toluene rinse was used to wash away the excess surfactant and polymers on the surface, followed by thermal annealing at 120 °C for >1 h in the oven. After that, an xdi-dcs thin layer was printed (with sheath gas (SG) flow rate of 40CCM and printing speed (PS) of 10 mm s^{-1} as default settings) as the gate dielectric (xdi-dcs ink: Xerox Research Center Canada), which was diluted and optimized with natural $\geqslant$99.5% butyl alcohol (Sigma Aldrich) in appropriate percentage, and cured by thermal annealing at

140 °C for 20 min in the oven. Then, 2–3 min oxygen plasma was applied to make the xdi-dcs surface hydrophilic again before Ag printing to fabricate gate electrodes on top, followed by Ag curing at 150 °C for 15~25 min. The ultrasonic atomizer (UA) is good enough for the printing of all inks involved. The smallest channel length achieved was ~20 μm. The SG flow rate, UA flow rate and PS were chosen differently to control the printing quality with respect to different inks. The additional fabrication details can be found in the supporting information (figures S1–S4, which is available online at stacks. iop.org/NANO/31/235301/mmedia). Figure 2 describes the structure and scanning electron microscope (SEM) images of the printed CNT-TFTs.

3. Results and discussion

For comparison, CNT-TFTs with ~80 nm aluminum oxide (Al_2O_3) layer as the gate dielectric were fabricated using ALD at 100 °C, replacing the xdi-dcs layer for new CNT-TFTs (ALD-based CNT-TFTs), as depicted in figure 2(c) (the rest of the fabrication steps are the same). CNT network is printed on top of the S/D electrodes, which is shown to have better contact than S/D on top of CNT network [20]. Top gate is used in the CNT-TFTs to achieve lower hysteresis (figure S5 of supporting information) of the devices, as CNT network is not in direct contact with the environment. The morphology of the CNT-TFTs (as-printed Ag, CNT network and xdi-dcs) on flexible substrates can be seen in figure 2(b). CNT network is only visible by using SEM. Figure 2(b) (the middle) shows uniform CNT network resulting from the layer-by-layer deposition method, i.e. CNT printing, toluene rinsing and blow dry processes (one cycle altogether) are performed
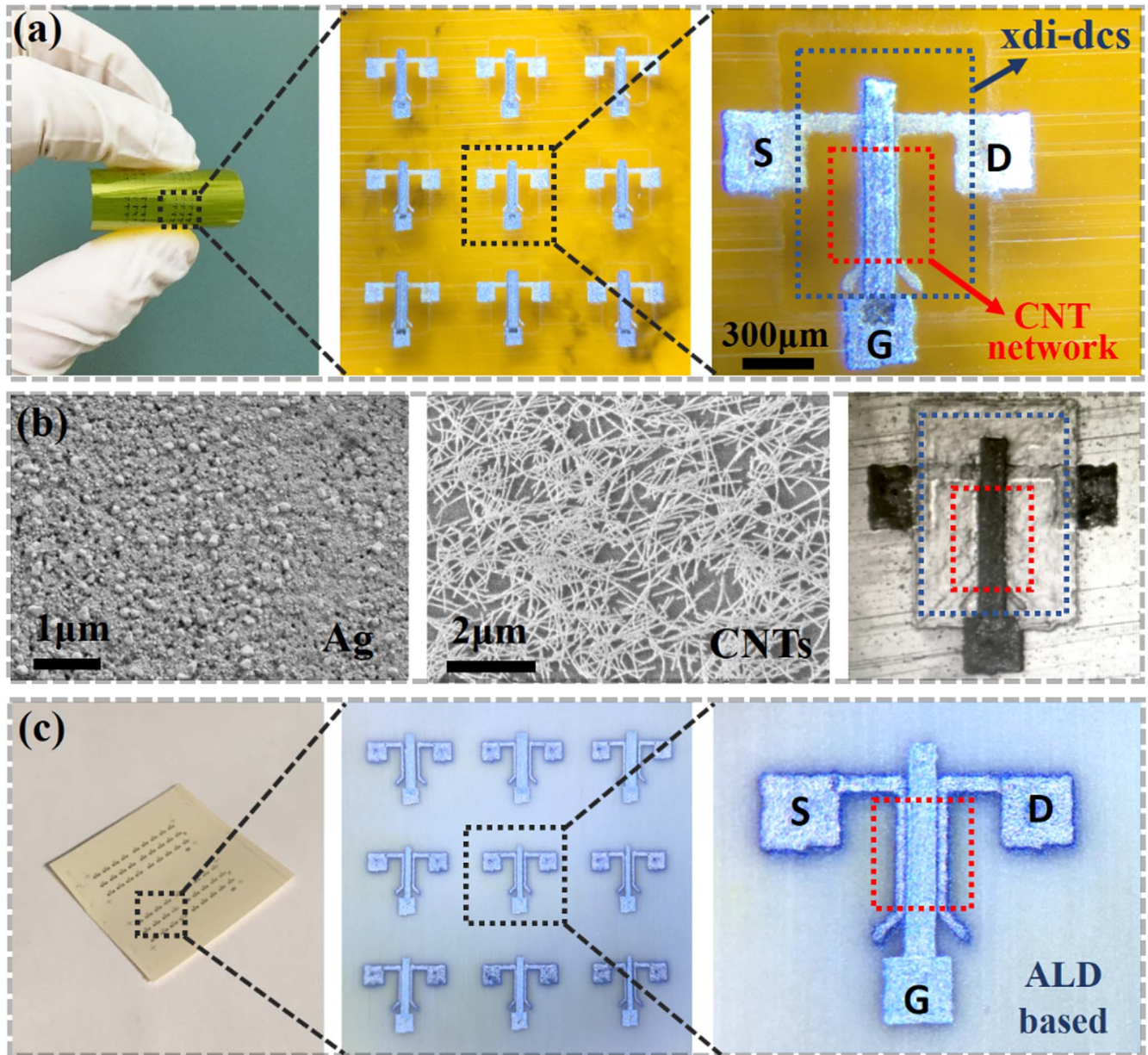
Figure 2. Features and morphology of printed CNT-TFTs. (a) Fully printed CNT-TFTs on Kapton substrate using xdi-dcs dielectric layer. xdi-dcs layer is a transparent thin film under the microscope where the CNT network (denoted by red dash box) is almost invisible in the channel. (b) SEM images show morphology of Ag electrodes, CNT network and a CNT-TFT. (c) Printed CNT-TFTs on LCP substrate using ALD dielectric layer.

repeatedly for density control and to deposit highly uniform CNT network (normally 2∼4 cycles). The significance of oxygen plasma treatment and layer-by-layer deposition on CNT network uniformity can be observed in figure 3. Without oxygen plasma, CNTs tend to bundle together because of the hydrophobic nature of the surface. Thus, the corresponding network is non-uniform and it is hard to control the density. After the treatment, density control can be achieved through layer-by-layer deposition, which is more efficient than density control by using different concentration of CNT solution. Similar improvement is also achieved for Ag printing on top of xdi-dcs thin film.

The performance of fully printed CNT-TFTs is mainly limited by the gate dielectric. The printing of a xdi-dcs thin film is critical to obtain relatively high-performance CNT-TFTs. During AJP printing, the thickness of xdi-dcs can vary in a broad range based on the dilute ratio of xdi-dcs as well as the printing parameters such as the SG flow rate, UA flow rate and PS. For a given SG/US/PS combination, the thickness variation (as shown in figure S4) can result from various factors such as the stability and accuracy of the AJP printer, the surface quality of the substrate or previously printed features, the curing process of the dielectric layer, etc. All these factors should be considered, while attempting to reduce the dielectric thickness (330 ± 140 nm), to avoid the failure of the dielectric layer during device fabrication. The thinnest xdi-dcs film we achieved for a CNT-TFT is ~ 0.3 μm (SG = 18CCM and PS = 10 mm s^{-1} as default setting unless
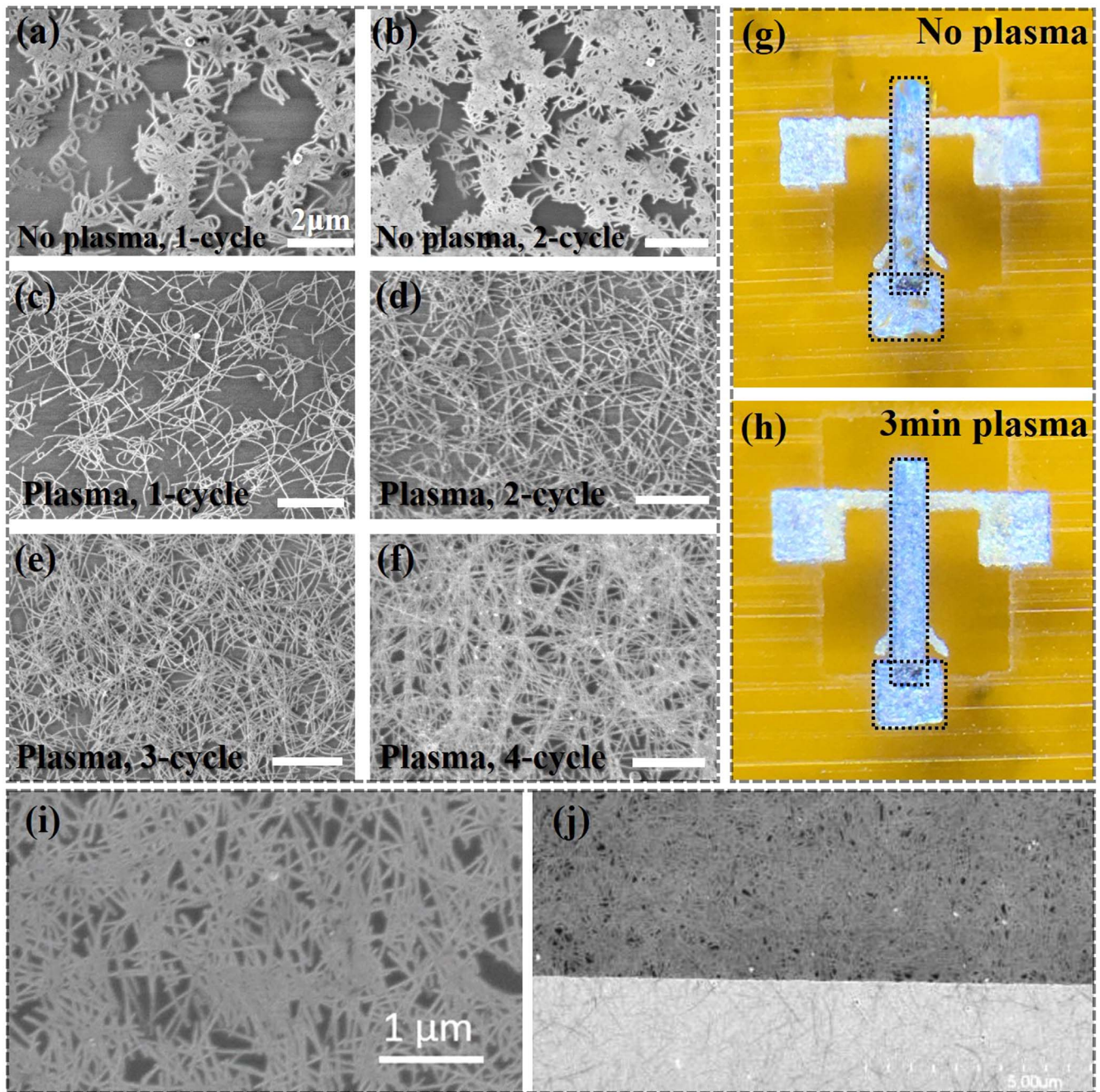
Figure 3. Effects of oxygen plasma treatment before CNT network printing (a)–(f) and Ag printing (g)–(h) on top of xdi-dcs thin film. Without plasma treatment, CNTs bundle together easily (a)–(b) and Ag thin film is uneven with huge pinholes everywhere (g). CNT network density can be well controlled by layer-by-layer deposition after plasma treatment (c)–(f). Scale bar is 2 μm in (a)–(f). (i) and (j) are the SEM images from [31] and [36], respectively, the densities of which are much higher than in (c)–(d). Improvement in printing conductive single layer of CNT network (very low density) results in the increase of on/off ratio of the fully printed CNT-TFTs.

stated otherwise, UA flow rate = 30CCM in this case), and the thickest is close to 1 μm (measured by Tencor P15 profilometer). Figure 4 displays the difference in transfer characteristics caused by the thickness of xdi-dcs thin film. The difference in thickness is controlled by the values of UA flow rate, which are 30, 32 and 36CCM for 0.33, 0.41 and 0.59 μm, respectively. Except for the values of UA flow rate, the fabrication process and other parameters/dimension are exactly the same for the CNT-TFTs (W = 500 μm, L = 100 μm, 2-cycle CNT network deposition). Figure 4(a)

compares the transfer curves of fully printed CNT-TFTs with different thickness of dielectric layers. It is clear that the range of V_g needed to fully switch on and off the devices depends on the thickness of the printed xdi-dcs layer. As observed from the figure, for the device with thickness of 0.33 μm, the V_g has to be swept between $-8\sim6$ V in order to reach an on/off ratio of 10^5. However, the V_g has to be swept in the range of $-10\sim16$ V in order to switch on and off the device with thickness of 0.59 μm. Obviously, the thicker the printed dielectric layer, the larger the V_g needed for the transistor to
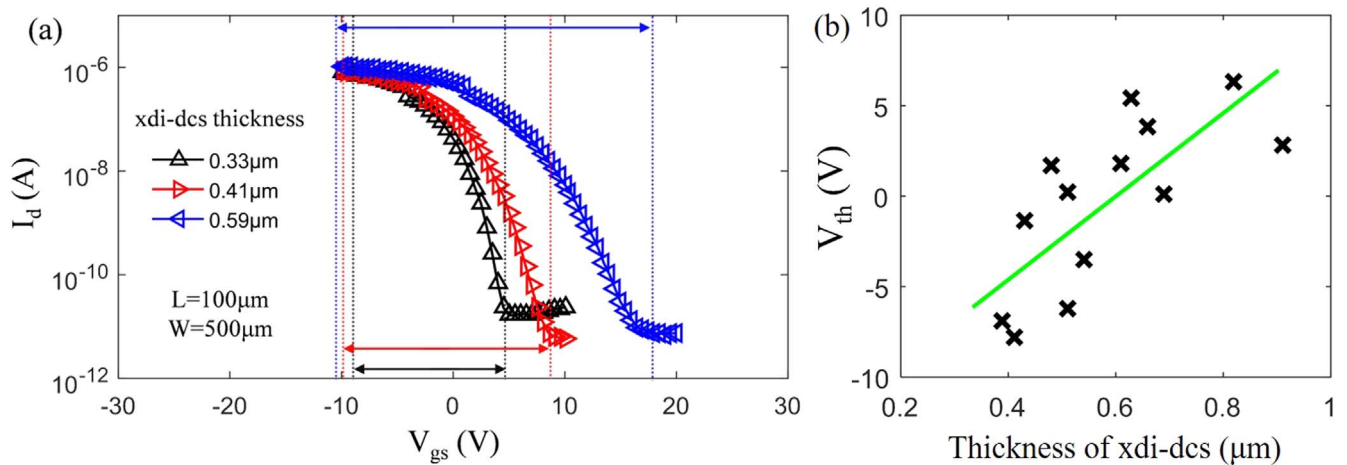
Figure 4. Impact of the printed xdi-dcs layer on the performance of fully printed CNT-TFTs. (a) Comparison of transfer curves of three fully printed CNT-TFTs with different thickness of dielectric layers. (b) Dependence of V_{th} on the thickness of printed xdi-dcs thin films for fully printed CNT-TFTs.

Table 1. Performance comparison and fabrication details of printed CNT-TFTs in the literature. Generally, an ALD-based device has better performance and stability, but the cost is high. Ion-gel-based devices can achieve low operation voltage, but are physically fragile. This work achieved better performance for fully printed flexible devices using xdi-dcs as the dielectric based on the single printing method (In [36], fabricated devices are not based on a single printing method and most of the data is for devices fabricated on hard substrate). The references with asterisks ([33], [42] and [36]) denote the usage of an encapsulation layer for the back-gated devices.

Reference	Operation voltage V_g	Hysteresis	Best on/off ratio	Fully printed	Dielectric	Fabrication
*[33]	~4 V	~0.6 V	~10^4	No	ALD based	IJP/photolithography
[40]	~6 V	~3.8 V	>10^5	Yes	ion gel	Gravure with masks
[28]	~1.5 V	~0.4 V	>10^5	No	ion gel	AJP/photolithography
[43]	~1 V	~0.1 V	N/A	Yes	ion gel	IJP
[41]	~20 V	~5 V	<10^4	Yes	BaTiO$_3$/PMMA	IJP-like
[30]	~30 V	~4 V	<10^4	Yes	BaTiO$_3$/PMMA	Printing with masks
*[42]	~15 V	~0.03–0.45 V	~10^4	No	xdi-dcs, Teflon-AF	Spin coat/AJP based
[31]	~40 V	~0.5 V	~10^5	Yes	xdi-dcs	AJP
*[36]	~5 V	~0.2 V	>10^4	Yes	BaTiO$_3$	IJP/R2R
This work	~6 V	~0.6 V	>10^5	Yes	xdi-dcs	AJP

operate at its highest on/off ratio. This is because the gate capacitance is directly related to the thickness of the dielectric, which affects the transconductance of the transistors. Figure 4(b) plots the dependence between the thickness of the printed xdi-dcs layer and V_{th} for a set of fully printed CNT-TFTs (each cross denotes a different CNT-TFT). These CNT-TFTs were fabricated using the same process and parameters, except that the PS value is different in order to control the thickness of the xdi-dcs layers. Generally, a positive correlation can be seen from the plot, i.e. if the printed dielectric layer is thicker, the transistor tends to have a higher value of V_{th}. However, it is very difficult to obtain a one-to-one relationship between the thickness of the printed xdi-dcs layer and V_{th} because V_{th} also depends on other factors such as operation temperature, charges in dielectrics, etc (which is hard to control for state-of-the-art printed CNT-TFTs, even though they are fabricated exactly the same way). The xdi-dcs thin film with thickness less than 0.3 μm can easily cause a short between the gate and S/D electrodes, while an over-printing can appear with ink spill outside the designed feature

when the thickness is larger than 1 μm, which should be avoided. Table 1 compares the performance (both hysteresis and operation voltage V_g) of some printed CNT-TFTs in the literature, which were fabricated using different printing methods. It is clear that ion-gel-based devices have better performance compared to the rest, but printed ion gel could compromise the long term stability of the transistors because of its inherent fragility. ALD-based devices [33] are not fully printed, which will increase the fabrication cost. The performance of polymer-based devices ([36–41] uses a combination of printing methods for fabrication) varies largely depending on the fabrication method and dielectric material used. Compared to other polymer-based devices, especially considering fully printed CNT-TFTs, the devices in this work have the obvious advantage of low operation voltages because of the improvement in xdi-dcs-based dielectric layer. And the improvement in the uniformity of the CNT network results in very high on/off ratio of the fully printed devices.

Even though a thin xdi-dcs layer is the key for fully printed CNT-TFTs, it is difficult to print films thinner than
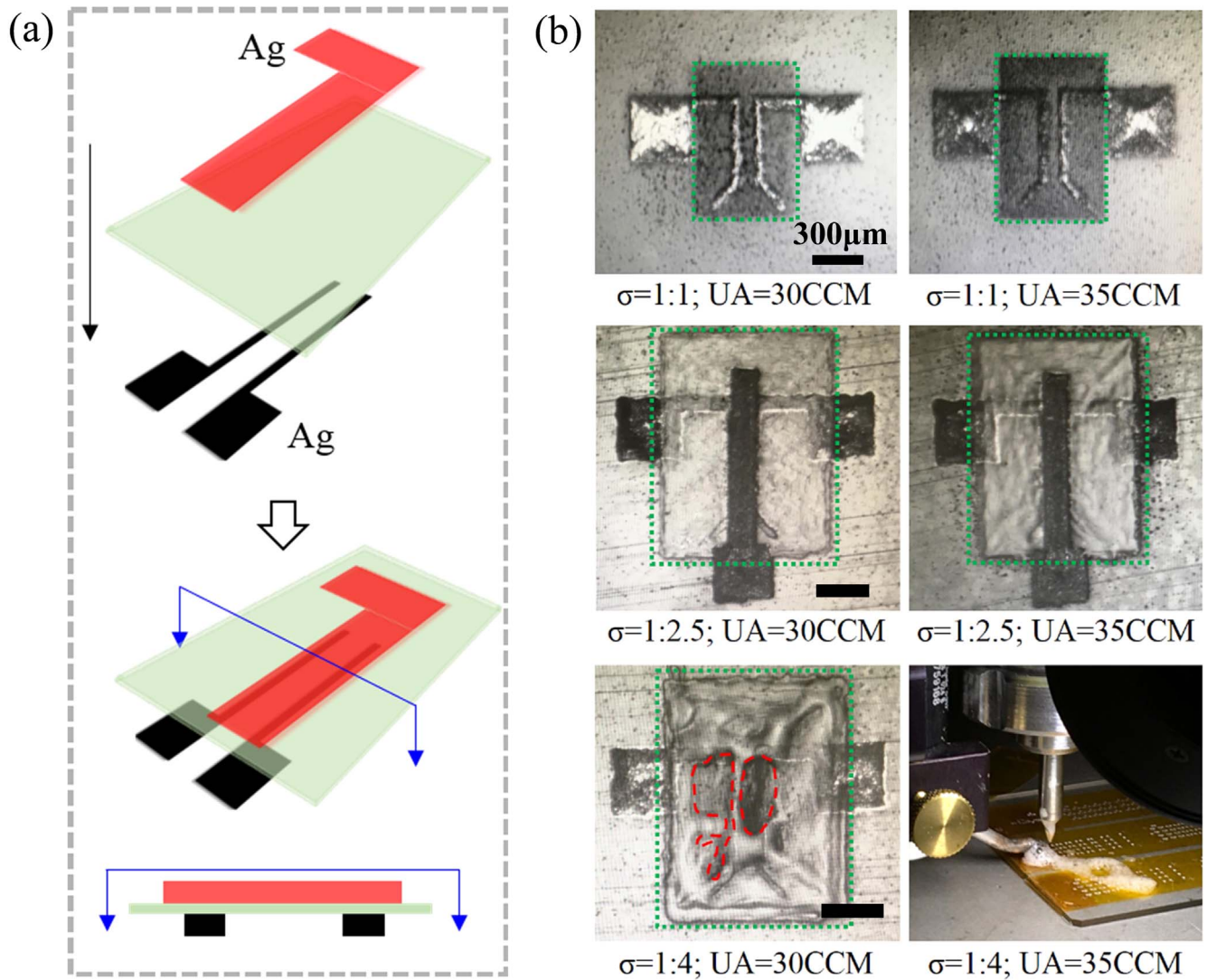
Figure 5. (a) Schematic structure (layer-by-layer structure and the sectional view) used to test the insulation quality of printed xdi-dcs thin films (light green layer). (b) Visualization of printed xdi-dcs thin film at different dilute ratio σ (1:1, 1:2.5 and 1:4) and UA flow rate (30 and 35CCM). Thin films in higher figures will not work well for devices, as numerous pinholes are present because of the particle-like behavior during xdi-dcs printing. That means the concentration of dielectric ink is still too high, since σ is only 1:1. The middle figures show well-printed xdi-dcs thin films. No pinholes exist when σ is 1:2.5 and the thickness of the printed dielectric layers can be controlled by the UA flow rate. Thin films in lower figures will not work either because of the overprinting, which can result in several big pinholes (denoted by the red dash area, left) and even ruin the substrate (right). That means the concentration of dielectric ink is still too low when σ is 1:4. All scale bars are 300 μm.

0.3 μm because the pinholes in such thin films (<0.3 μm) can easily cause a short circuit in the TFT ($\sim$pinhole effect, which fails to provide insulation between the gate and S/D electrodes). Figure 5(a) illustrates the structure we used to test the insulation quality of printed xdi-dcs thin film, which is similar to the structure in fully printed CNT-TFTs. Undoubtedly, good insulation (leakage current $\ll$0.1 nA) of the printed dielectric is a precondition for fully printed CNT-TFTs. The measured capacitance of printed xdi-dcs thin film is in the range of 6–8 nF cm^{-2} with thickness changing from 0.8 to 0.3 μm, respectively. Generally, the poor quality of the xdi-dcs layer results from the severe pinhole effect when current can flow directly from the gate electrode (red electrode in figure 5(a)) to the S/D electrodes ($\sim$black electrodes in

figure 5(a)). To optimize the quality of the printed xdi-dcs layer, natural $\geqslant$99.5% butyl alcohol is used to dilute the xdi-dcs ink with a dilution ratio σ (defined as volumetric ratio of xdi-dcs : butyl alcohol) ranging from 1:1–1:4. Figure 5(b) shows the printed xdi-dcs layers at different σ and UA flow rate, which are the two key parameters to control the quality of printed xdi-dcs thin film. As shown in this figure, when σ is 1:1 corresponding to low dilution, continuous thin layer cannot be formed. Instead, the printed features show particle-like morphology with numerous small pinholes. When σ is 1:4, the morphology of the printed features is highly uneven with several large pinholes (red dash area in figure 5(b)). When the UA flow rate is as large as 35CCM, overspill of the ink from the nozzle will ruin the substrate (overprinting).
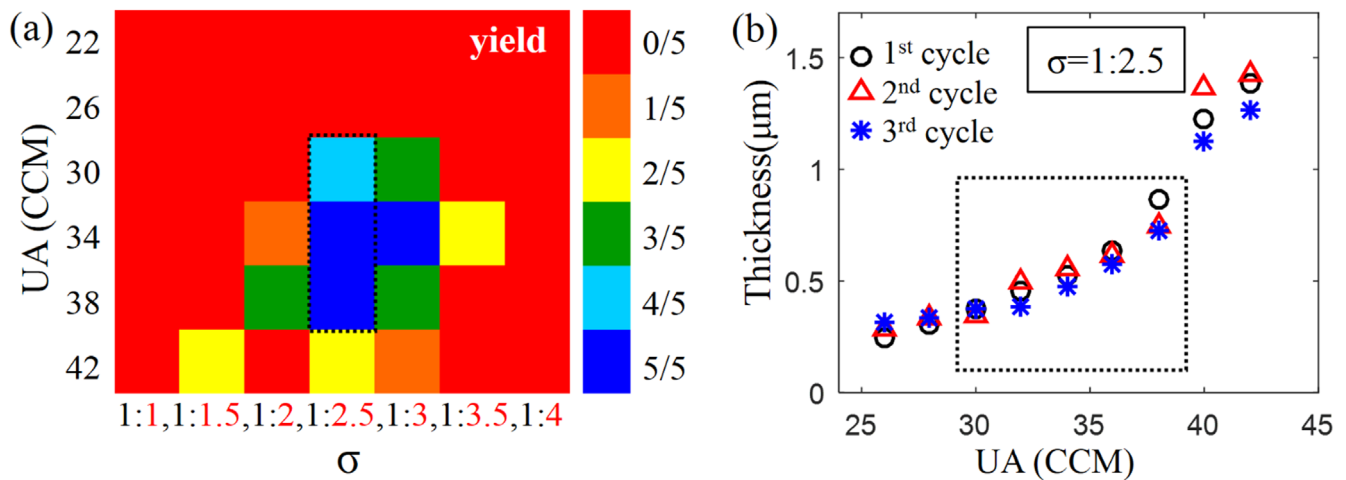
Figure 6. Optimization of printed xdi-dcs thin film. (a) Yield rate (number of samples with good insulation quality that have leakage current much less than off current of the corresponding transistors ∼0.1 nA) under different σ and UA flow rate combinations. (b) Thickness dependence of xdi-dcs thin film on UA flow rate when σ is equal to 1:2.5, which is the best σ from (a). Black dash box in (a) and (b) denotes UA flow rate range of 30–38CCM at best σ.

Clearly, overprinting of xdi-dcs can cause additional problems. In general, good morphology of printed features can be achieved when σ is around 1:2.5, which results in very uniform and continuous xdi-dcs thin film and the thickness can be well controlled by changing the UA flow rate accordingly.

Based on the structure displayed in figure 5(a), five samples are fabricated for each combination of σ and UA flow rate, with σ varying from 1:1 to 1:4 and the UA flow rate varying from 22–42CCM. Numerator/denominator format is used to describe the results. When the denominator equals 5, it denotes the result is for a specific σ and a specific UA flow rate. When the denominator equals 30, it denotes the result is for a specific σ and all UA flow rates. The yield counts the number of samples without shorting between the red Ag electrode and the two black Ag electrodes with printed xdi-dcs in between. The results can be seen in figure 6(a). The yield rates of the samples with good insulation quality are 0/30, 2/30, 4/30, 16/30, 12/30, 2/30 and 0/30 (denominator is the number of all samples; numerator is the number of good samples) when σ is equal to 1:1, 1:1.5, 1:2, 1:2.5, 1:3, 1:3.5 and 1:4, respectively, with the UA flow rate changing from 22 to 42CCM for each σ. Similarly, those values are 0/30, 0/30, 7/30, 13/30, 11/30 and 5/30 when the UA flow rate is equal to 22, 26, 30, 34, 38 and 42CCM, respectively, with σ changing from 1:1 to 1:4 for each UA flow rate. Therefore, (σ, UA flow rate) = (1:2.5, 34), would be one of the best combinations for the printing of xdi-dcs thin film. Other combinations such as (σ, UA flow rate) = (1:2.5, 38) and (σ, UA flow rate) = (1:3, 34) are also very reliable in the test. The value of σ is more important because it cannot be adjusted freely during printing, and should be determined before printing. Figure 6(b) plots the thickness dependence on UA flow rate of printed xdi-dcs thin film when σ is determined as 1:2.5 in advance. The UA flow rate can be changed freely as needed during printing. To guarantee the stability of

the ink mist of xdi-dcs, the printing is performed 2 min after the changing of the UA value. The time interval for each printing cycle (1st, 2nd and 3rd cycle) is roughly 1 h. Generally, the dependence in figure 6(b) should be linear because of mass conservation. However, the printing becomes unstable when the UA flow rate > 40CCM (σ = 1:2.5). Overprinting can happen when the UA flow rate is close to 50CCM, which is similar to that depicted in figure 5(b) when (σ, UA flow rate) = (1:4, 35). The data inside the black dash box of figure 6(b) corresponds to the high yield rate, which can be observed in figure 6(a). Collectively, the thinnest xdi-dcs film is around 0.3 μm in fully printed CNT-TFTs. By optimizing the printing process without shorting of electrodes, it can enable on and off switching using V_g below ±10 V.

The *I–V* characteristics of the CNT-TFTs were measured using a Microtech Summit 11 k probe station and Keithley 4200 SCS. We fabricated a series of devices with the same channel width (W = 500 μm), but different channel lengths (L = 50∼250 μm). The output characteristics (I_d−V_{ds} curves) and the transfer characteristics (I_d−V_{gs} curves) of the CNT-TFTs are plotted in figure 7. Figures 7(a) and (b) are ALD-based CNT-TFTs, while figures 7(c) and (d) are fully printed CNT-TFTs. The on/off ratio of the fully printed CNT-TFTs ranges from 10^3–10^6, which increases with increasing channel length because of lower probability for metallic CNTs to form a conductive path. The random CNT network can also cause difference in the on/off ratio. The overall *I–V* characteristics show p-type performance with mobility ranging from 2–8 cm^{2}V^{-1}s^{-1}.

4. Conclusions

Fully printed CNT-TFTs have been fabricated on flexible substrates using AJP. The fabricated devices can be fully switched on and off using V_g below ±10 V to reach on/off ratio as high as ∼10^5. Single layer and multiple layers of
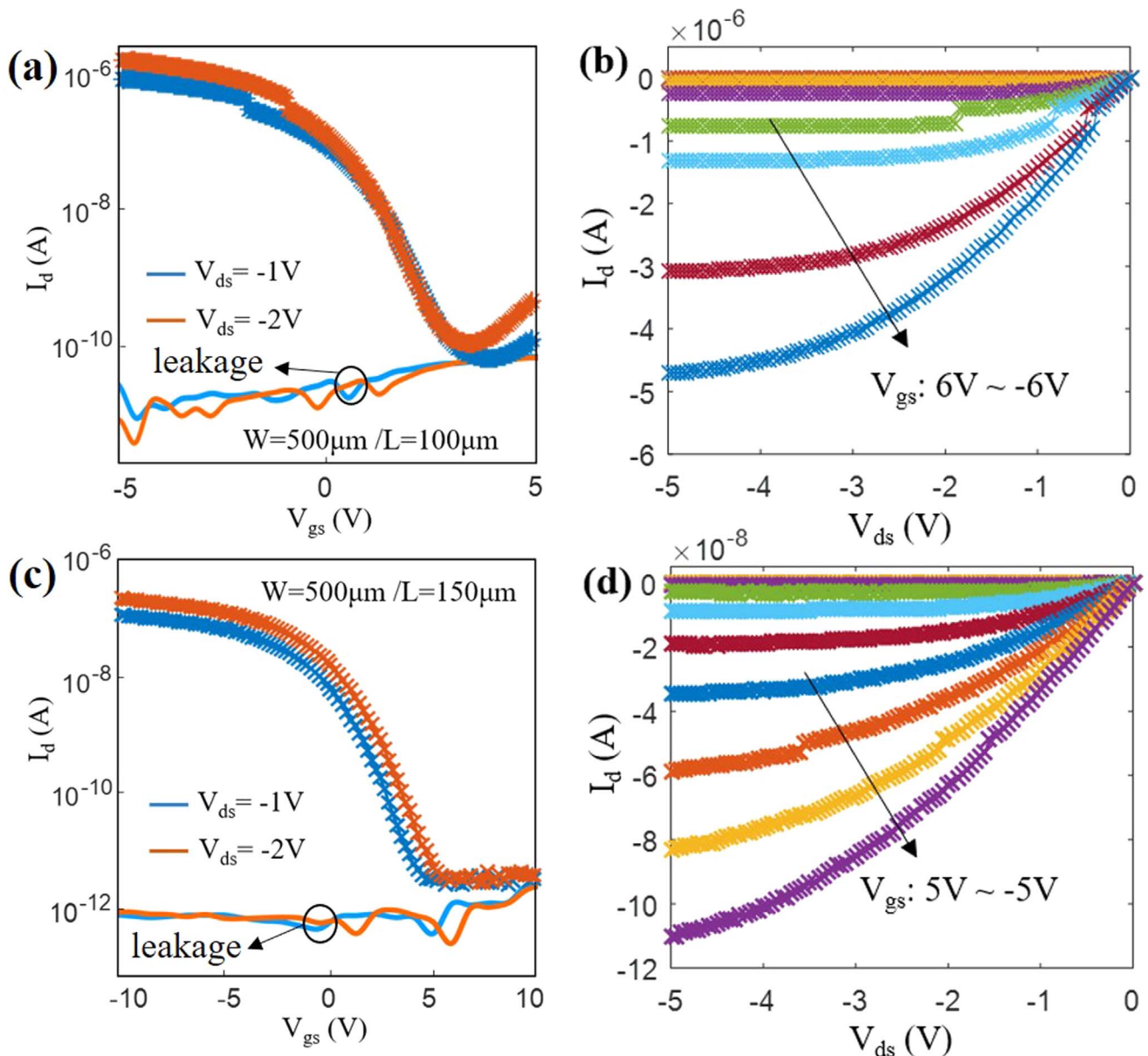
Figure 7. *I–V* characteristics of CNT-TFTs. Transfer curve (a) and output curve (b) of an ALD-based printed CNT-TFT (∼80 nm Al₂O₃, W = 500 μm, L = 100 μm, 1-cycle CNT network deposition). Transfer curve (c) and output curve (d) of a fully printed CNT-TFT based on printed dielectric layer with thickness as small as 0.3 μm (W = 500 μm, L = 150 μm, 3-cycle CNT network deposition).

CNT network are printed and analyzed, which facilitates density control as well as highly uniform CNT network structure. By diluting xdi-dcs with natural (⩾99.5%) butyl alcohol in appropriate volumetric ratio (σ = 1:2.5), printed dielectric thin film with thickness of ∼0.3 μm is achieved in fully printed CNT-TFTs. A high-quality printed dielectric layer free of the pinhole effect is demonstrated with high yield rate by controlling the UA value. The achieved improvement in the printed dielectric layer is crucial for lower-voltage operation of flexible transistors and lower power dissipation, which paves the way for the employment of CNT-TFTs as building blocks in flexible wearable devices such as high-performance displays, RFID tags, sensors, artificial skin, etc.

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