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Experimentally calibrated electro-thermal modeling of temperature dynamics in memristors

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ABSTRACT

As nanoscale electronic devices are being packed into dense three-dimensional arrays, the effects of the thermal environment of the system during device operation become critical, but are not clearly understood. Predicting the temperature evolution using a robust model will provide critical design guidelines for complex memory and computing systems. Here, we used in-operando thermal and x-ray mapping with sub-micrometer spatial and sub-microsecond temporal resolutions on functioning tantalum oxide memristive switches and observed hot spots corresponding to oxygen concentration gradients, indicating the presence of localized conductive filaments. We constructed a hybrid electro-thermal model comprising 3D heat transfer and 0D resistive switching models to predict electrical characteristics and the temperature rise and calibrated it against the measurements. We also demonstrated thermal crosstalk in an array of memristors to illustrate localized heating. Such a model will guide system design by considering thermal performance, which is critical to most future electronic chips.

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Resistive random access memory (RRAM) has garnered increasing interest among researchers due to its low power operation,[1] promising scaling,[2] and fast switching.[3] Two-terminal nonvolatile memory or memristors such as resistive random access memory and phase change memory can be good candidates for the next-generation storage technology and to solve the scaling challenge faced by the charge-based storage technology.[4] The resistive switch is also promising for neuromorphic computing,[5–8] which can benefit many deep learning applications.

RRAM is a two-terminal device and turns on and off by forming and rupturing conductive filaments between electrodes.[9–14] The conductive filaments are made of oxygen vacancies for valence change memory (VCM) and cations for electrochemical metallization memory (ECM). Electroforming is needed for a fresh resistive switching device to form filaments.[15] In the case of bipolar resistive switch VCM, the device can change from the high resistance state (HRS) to the low resistance state (LRS) when a positive bias is applied, which is called the set process. A low resistance state device can become high resistance state when a negative bias is applied, and this is called the reset process. The movement of the oxygen vacancies can be driven by the electric field, concentration gradient, and temperature gradient through drift, Fick diffusion and thermophoresis during both set and reset processes.[16,17] Fick diffusion moves the oxygen vacancies from the high concentration region to the low concentration region, making the concentration inside the filament lower. Conductive filaments generate a large amount of heat under voltage bias, which makes filaments hotter than the surrounding insulating material. The resulting temperature gradient makes the oxygen vacancies move toward the filaments under the Soret effect.

Temperature plays an important role in RRAM operation,[18–21] e.g., in HfO_x- and TaO_x-based devices, both of which are promising for memristors. The I–V characteristics of set-reset processes of the TaO_x memristor could be explained by Mott hopping and Schottky emission.[20] The electrical conductance due to Schottky emission is dependent on temperature.[20] The dynamics of the oxygen vacancy like drift, diffusion, and thermophoresis[16,17] can also be affected by temperature. Therefore, the change of temperature during device operation will significantly influence the resistive switching process, which has been observed in experiments on HfO_x-based memristors.[18,19] An experimental study found that the on-off resistance ratio of TiN/HfO_2/Ti/TiN memristors decreases with increasing temperature.[18] Another study reported that the resistance of the Au/Ti/HfO_x/Au

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device in the LRS could be higher when using a thermally conductive substrate.[19] Knowing the temperature of memristors is important to understand their working mechanism, build more accurate computational models, and assist device design with proper thermal management. Device temperature can be affected by device design and thermal conductivity of materials, and the thermal conductivity of HfO_x and TaO_x has been measured by time-domain thermoreflectance method.[22–24] Although the internal temperature of the TaO_x resistive memristor could be as high as 750 K–1000 K according to the numerical simulations [17,25] and the temperature of NbO_2 threshold switches has been shown to be more than 1200 K through thermoreflectance-based temperature mapping,[26] the temperature of resistive switches during operation has not been directly measured by the previous experimental studies. The present study takes an important step in measuring the temperature of TaO_x memristor devices during operation.

Commercial implementation of RRAM requires a high density of devices, making it essential to properly evaluate and avoid the effect of thermal crosstalk between devices. For the design of the crossbar structure, units in the same row or column share the same electrode lines. The electrode line usually has high thermal conductivity and can transport heat efficiently from one device to its neighboring devices.[21] Computational models that consider 3D thermal environment of a device will serve as a good tool to evaluate the thermal behavior, but the multi-physics models developed for simulation of devices are either computationally expensive or oversimplified and do not consider the effect of devices located nearby. Models that consider the vacancy drift and diffusion [27,28] involve solving coupled partial differential equations (PDEs) and are able to simulate 2D structures but would take a very long time to simulate 3D structures with multiple devices. Simpler models, such as 1D models, considering only the size of filaments can do fast predictions,[29] but the 3D thermal environment is not considered and, therefore, not suitable for system-level simulation.

In this study, temperature profiles of TaO_x memristors during operation were measured by an ultrafast thermoreflectance-based thermal imaging system. The temperature rise on the electrodes of device subjected to voltage pulses corresponding to a set-reset process was measured. An electro-thermal model that can simulate resistive switching of multiple devices in a 3D geometry was developed and validated against the experimental results. The developed model can be extended to simulate a system with multiple memristors.

The schematic of TaO_x devices investigated in this work is shown in Fig. 1(b). The top electrode and bottom electrode are 20 nm thick Pt. The switch unit between electrodes has a lateral size of 5 μm by 5 μm and consists of 6 nm thick Ta and 8 nm thick TaO_x. The entire device is placed on a 200 nm thick Si_3N_4 membrane, which is suspended in air.[16] Suspending the devices creates thermal isolation and leads to higher temperature rise. Temperature was measured by a thermoreflectance-based system[30] shown in Fig. 1(a). In this setup, the temperature change at a surface is assumed to be linear to the reflectance change, which can be captured by a charge coupled device (CCD) camera. We used a 530 nm light emitting diode (LED) light source since the thermoreflectance coefficient at this wavelength is high for our samples. A 100x magnification lens was used, providing ~290 nm spatial resolution. Transient temperature was measured by delaying the LED pulses with respect to the applied voltage pulses, as

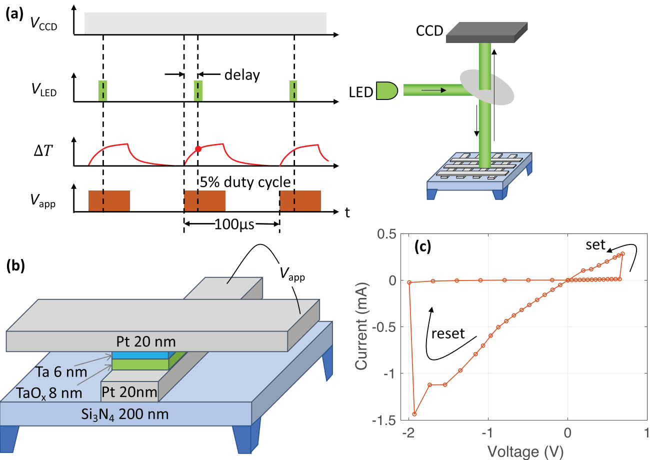

FIG. 1. Schematic of the crossbar device and temperature measurement system. (a) Schematic of the thermoreflectance-based temperature scanning system. (b) Pt/Ta/TaO_x/Pt crossbar device on the Si_3N_4 membrane. The device is suspended in air. (c) Measured current–voltage curve for a TaO_x device, where each data point was obtained by measuring the current in response to voltage pulses.

indicated by the schematic in Fig. 1(a). The temperature profile was averaged over multiple periods to improve the signal-to-noise ratio.

The experimental setup was prepared for quasi-static voltage sweeping and temperature was measured by applying voltage pulses (see the supplementary material for details). Electro-forming was performed to a fresh device by applying large voltage bias with current compliance, followed by several loops of set and reset with quasi-static voltage sweep. Averaging the temperature signal is necessary to increase the measurement accuracy. Voltage pulses of 100 μs period with a 5% duty cycle were used to operate the device when measuring temperatures. A current–voltage curve measured by applying voltage pulses is shown in Fig. 1(c). The set operation gradually changed the amplitude of positive voltage pulses and follows the order of 0 V → 0.7 V → 0 V. The reset process is similar to the set process, except that it applied negative voltage pulses follows the order of 0 V → −2.0 V → 0 V. Each point was averaged over a series of voltage pulses after the state was stabilized at specified voltage. It can be observed from the current-voltage curve that the device was turned on at 0.7 V and turned off at −2.0 V. The device can function normally after the temperature measurement, as confirmed by the I–V test with quasi-static voltage sweep.

The TaO_x device showed localized Joule heating under the voltage bias in the low resistance state as shown in Figs. 2(a)–2(e) for the set process and Figs. 2(f)–2(j) for the reset process. The temperature profiles shown in Figs. 2(a)–2(j) were measured at the end of 5 μs voltage pulses. For the set process, the voltage pulse amplitude increased from 0 V to 0.7 V and then decreased to 0 V. There was no obvious localized Joule heating until the voltage increased to 0.7 V. This is consistent with the current measurement, indicating that the device was set at 0.7 V and localized filaments were formed at that voltage bias. Once the device was set, the filaments remained conductive until the device was reset. The hot spot at the left bottom corner indicates the location of filaments. Note that filaments could have various sizes in the range between a few nanometers to hundreds of

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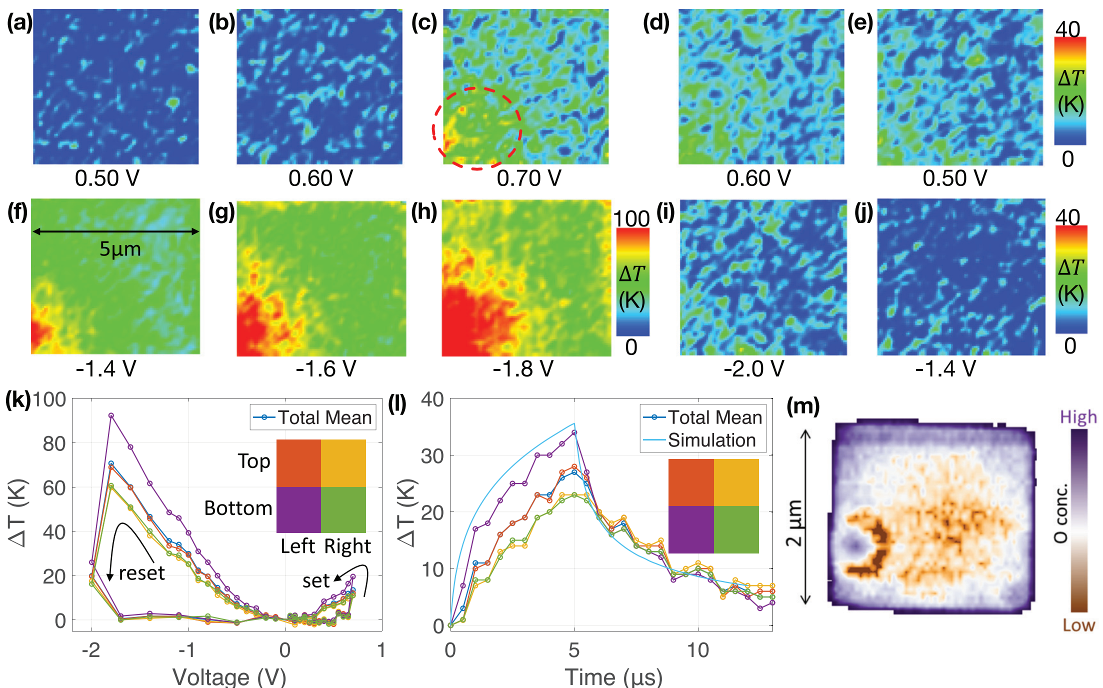

FIG. 2. Temperature distribution and oxygen concentration in a crossbar device subjected to voltage pulses and (a)–(j) temperature contours indicating temperature rise measured at the end of 5 µs voltage pulses during the set and reset processes. The set process applied positive voltage pulses whose amplitude followed the order of 0 V → 0.7 V → 0 V. The reset process applied negative voltage pulses whose amplitude followed the order of 0 V → −2.0 V → 0 V. The temperature plots in figures (a)–(j) correspond to the set process followed by the reset process. The device was in the high resistance state in [(a)–(b) and (i)–(j)] and in the low resistance state in (c)–(h). The red dashed circle in (c) highlights the localized hot spot due to Joule heating. [(a)–(e) and (i)–(j)] use range 0 K–40 K for temperature color maps, and (f)–(h) use range 0 K–100 K. (k) Temperature rise at the end of 5 µs voltage pulses for four evenly split regions of the device; split regions are illustrated in the inset. (l) Temperature rise vs time at −1.0 V (LRS) from a crossbar device. Temperature at the bottom left quarter simulated using a hybrid model developed in this study is also shown. (m) Oxygen concentration map of a crossbar device in the LRS.

nanometers;[15,16] therefore, the device may have one or multiple filaments and most of the filaments were at the left bottom corner. The Joule heating in the device in the low resistance state was obvious for positive voltages higher than 0.3 V, below which the heating power may be very low to increase temperature significantly. During the reset process, negative voltage pulses were applied whose amplitude was changed from 0 V to −2.0 V and then changed back to 0 V. From Figs. 2(f)–2(j), it can be inferred that the localized heating existed before the voltage reaching −2.0 V, at which point the device was reset and filaments ruptured. The temperature rise was negligible in the high resistance state compared to the LRS at the same voltage.

The temperature was not uniform across the lateral surface of the device as observed through hot spots in Fig. 2 because the filaments inside the tested device may have different sizes and the conductive region was not uniformly formed. The location and size of filaments were mostly determined during the electro-forming process, which could be partially stochastic due to the nature of amorphous material but also depends on the material uniformity and morphology at the device junctions. The maximum temperature rise detected on the electrodes was 147 K when the device was in the LRS and applied voltage was −1.8 V. Although the temperature was measured at the surface, the electrode pad is thin and the measured temperature is expected to be close to the temperature at the TaO_x layer, which was confirmed by the numerical simulations (Fig. S2 in the supplementary material). However, the peak temperature rise inside the device could be much higher than the observed value of 147 K if the corresponding filament has a smaller size than the resolution of the temperature measurement (∼290 nm). In order to have a better understanding of the temperature distribution, the device is split evenly into 4 parts—top left, top right, bottom left, and bottom right, and the average temperature rise is evaluated for these parts and plotted in Fig. 2(k). It was consistently observed that at various voltage amplitudes, the bottom left corner has the maximum temperature rise and the two regions on the right have the lowest temperature rise. The average temperature rise at the bottom left region was 59% higher than that at the top right region on average for bias between −1.0 V and −1.8 V (LRS). The presence of the localized filament was also confirmed through the oxygen concentration map of a 2 µm × 2 µm crossbar device of the same batch measured by x-ray transmission, as shown in Fig. 2(m). The active region with a high oxygen content covers approximately around 20% of the device, similar to the portion of hot spots. The temperature would continue to rise if the voltage pulse was longer because the temperature had not reached the steady state at the end of 5 µs, as shown by transient temperature plots in Fig. 2(l). The temperature rise shown in Fig. 2(l) is from another device fabricated in the same batch. At the end of voltage pulses, the temperature in Fig. 2(l) is lower than in Fig. 2(h)

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due to higher electrical resistance. The temperature at the bottom left was consistently higher than the other regions during the heating process between 0 and 5 μs because lower resistance results in higher heating power. The temperature was similar in all regions just after the voltage was withdrawn at 5 μs. The thermal resistance R_{th} and thermal capacitance C_{th} are estimated to be 1.37×10^5 K/W and 1.68×10^{-11} J/K, by fitting the transient temperature at the bottom left quarter with a lumped heat transfer model. Since the temperature is local, the fitted R_{th} and C_{th} are estimates for the local thermal constants.

Evaluation of system-level thermal performance requires the capability of simulating heat transfer in a 3D structure and reflecting dynamics of state variables during the device operation. A hybrid electro-thermal model was developed to perform transient simulation. The hybrid electro-thermal model couples a 3D model for thermal analysis with a 0D model for resistive switching. The thermal model as explained in the supplementary material solves diffusive heat transportation and can handle different boundary conditions. Heat generation in the active region is assumed uniform and can be estimated from the current and voltage obtained by the electric model. The average temperature of the active region calculated by a 3D heat transfer model is assumed as the representative temperature of the active region and used as input to the 0D resistive switching model. The temperature in the active region is similar because the active region with filaments has higher thermal conductivity than the non-active region. The electric model solves ordinary differential equations (ODEs) considering current, voltage, and carrier density only for the active region. The active region is defined as the region with a high density of conductive filaments. For a device with one major active region, the device working conditions can be depicted by one set of I, V, and N. Here, I is the total current flowing through the device, V is the voltage between electrodes, and N is the average carrier density in the active region. This representation is reasonable when the goal is to investigate the operation of the entire unit rather than separate filaments. The current is contributed by Mott hopping and Schottky emission, which is able to explain measured current-voltage characteristics for both set and reset processes of TaO_x at different temperatures.[20] The current is a function of temperature, carrier density, and voltage, as shown in Eq. (1). Voltage and current are correlated by Ohm's law, as shown in Eq. (2). The dynamics of carrier density is dependent on both drift and diffusion, as shown in Eq. (3). The 3D thermal transport is governed by Eq. (4):

$$I = A_0 N T e^{\left(-\frac{E_{hop}}{k_B T} - \frac{2l}{\zeta}\right)} \sinh\left(\frac{lV}{d k_B T}\right) + A T^2 e^{\left(-\frac{\phi_{B0} - \beta\sqrt{V/d}}{k_B T}\right)} \tanh(V_1 V), \tag{1}$$

$$I = \frac{V_{app} - V}{R_{ser}}, \tag{2}$$

$$\frac{dN}{dt} = c_1 \left[\alpha_0 e^{\left(-\frac{E_{drift}}{k_B T}\right)} \sinh\left(\frac{T_1 |V|}{T V_0}\right)\right]^4 R_1(N) - p_0 e^{\left(-\frac{E_{diff}}{k_B T}\right)} R_2(N), \tag{3}$$

$$\frac{\partial T}{\partial t} = \alpha \nabla^2 T + \frac{\alpha}{k} q. \tag{4}$$

Here, l is the hopping distance, E_{hop} is the hopping energy, ζ is the wavefunction localization, d is the device thickness, ϕ_{B0} is the barrier height, R_{ser} is the overall series resistance including the resistance of contacts, electrode pads, and lines, p_0 is the prefactor for diffusion, V_{app} is the total voltage applied across the electrodes, N is proportional to the density of electrons multiplied by area, $\alpha = \frac{k}{c_p \rho}$ is the thermal diffusivity, k is the thermal conductivity, c_p is the specific heat capacity, ρ is the density, and q is the heat source. The tanh function is added to Schottky emission to capture nonlinearity. The drift term uses a combination of error functions in $R_1(N)$ to limit the range of N, as shown by Eq. (5). The diffusion term is linear to $R_2(N) = \max(N, n_4) - n_5$:

$$R_1(N) = \begin{Bmatrix} -c_2[0.5\,\mathrm{erf}(c_{n1}(N - n_1)) - 0.5\,\mathrm{erf}(c_{n2}(N - n_2))] & \text{for } V \le 0 \\ -c_3[0.5(\mathrm{erf}(c_{n3}(N - n_3)) - 1)] & \text{for } V > 0 \end{Bmatrix}. \tag{5}$$

The hybrid electro-thermal model can explain measured I–V curves and temperature while using proper constants. $A_0 = 2 l \nu_{ph} k_B$, $l = 0.25$ nm, $\nu_{ph} = 10^{13}$ Hz, $E_{hop} = 0.0038$ eV, $\phi_{B0} = 0.56$ eV, and $\beta = 2.5 \times 10^{-5}\ \mathrm{e}\sqrt{\mathrm{Vm}}$ were picked from Ref. 20. Simulation in this study uses $V_1 = 13\ \mathrm{V}^{-1}$, $T_1 = 300$ K, $A = 4.35 \times 10^{-7}\,\mathrm{A/K^2}$, $E_{drift} = 0.9$ V, $E_{diff} = 0.8$ V, $c_1 = 1.25 \times 10^{10}$ e/eVms, $c_2 = 10^{-15}$, $c_3 = 10$, $\alpha_0 = 5 \times 10^5 \exp((E_{drift} - 0.5\ \mathrm{eV})/(k_B T_1))$, $c_{n1} = c_{n2} = 10^9$ eVm/e, $c_{n3} = 10^8$ e/eVms, $n_1 = n_5 = 10^{-6}$ e/eVm, $n_2 = n_3 = 4.5 \times 10^{-5}$ e/eVm, $n_4 = 10^{-10}$ e/eVm, $V_0 = 0.7$ V, $p_0 = 10^{14}$ e/eVms, and $R_{ser} = 800\ \Omega$. Thermal conductivity for TaO_x is 4 W/mK in the active region and 1 W/mK for the non-active region.[24] Figure 3(a) shows the simulated I–V data. The simulation takes input of voltage pulse train similar to the experiments. The left bottom quarter was assumed to be the active region for the selected device since the hot spot was located in the left bottom region and temperature rise in other regions was due to heat diffusion, as confirmed by simulations. Five voltage pulses for each voltage amplitude were included, and each pulse has a period of 100 μs with 5% duty cycle. The model was not tuned to match the number of pulses needed to set and reset. The switching speed can be tuned by changing the constants in Eq. (3).

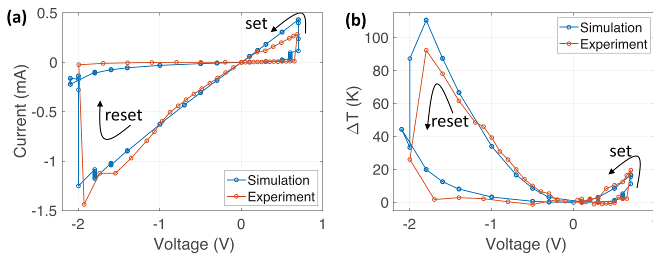

FIG. 3. (a) Current–voltage curve (b) temperature rise vs voltage obtained from simulations are compared against measurements. There were 5 pulses for each voltage. The voltage refers to the voltage applied across the electrode pads. The voltage and current values at the beginning and the end of each pulse are plotted. Temperature from the simulations is the value at the end of each voltage pulse and a transition bias like 0.7 V and −2.0 V may correspond to multiple values of temperature rise at the end of each voltage pulse. The temperature rise from the experiments is for the bottom left/active region. A bias of −2.1 V is included in the simulations in order to demonstrate that reset was finished at −2.0 V. The amplitude of pulsed bias for simulation was 0 V → 0.7 V → 0 V for the set process and 0 V → −2.1 V → 0 V for the reset process. The bias pulses have a period of 100 μs with 5% duty cycle.

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The conductance obtained from experiments at 0.2 V (LRS) was bit higher than at 0.3 V ~ 0.7 V (LRS) but was similar to −0.9 V ~ −0.1 V (LRS). Also, the conductance from experiments at −1.8 V ~ 0 V (HRS) was lower than at 0 V ~ 0.6 V (HRS), probably due to many negative pulses, which turned off the device. The model was tuned to match conductance at −1.8 V ~ 0.2 V (LRS) and 0 V ~ 0.6 V (HRS). The simulated temperature can closely match the experimentally measured average temperature for the active region at the end of 5 μs voltage pulse, as shown in Fig. 3(b). The temperature was slightly underestimated for −1.0 V ~ −0.3 V (LHS) and slightly overestimated for −1.8 V ~ −1.4 V (LHS). The tiny temperature difference between simulation prediction and experimental measurement was likely due to the assumptions made for the active region. For −1.8 V ~ −1.4 V (LHS), the conductance from simulation was underestimated, while the temperature was overestimated. A small amount of current might be contributed by the region assumed non-active, which means not all the Joule heating happened at the left bottom quarter. The model can also predict transient temperature pretty well, as shown in Fig. 2(i). The simulated temperature rises during 0–5 μs and temperature decay after power was withdrawn matches well with the experimental results.

Metallic lines dissipate most of the heat for the devices investigated in our work. The transient simulations of suspended devices indicate that at the end of 5 μs pulse, 21.63%, 21.53%, and 26.79% of generated heat were transferred out of the device through the left/right sides of the top electrode line, the north/south sides of the bottom electrode line, and the bottom surface of the bottom electrode, respectively. Electrode lines carry a major part of heat dissipation along the direction of metallic lines due to the superior thermal conductivity of Platinum. As the Si_3N_4 membrane is much thicker than other layers, heat spreading also occurs at the bottom surface of the bottom electrode.

The switching units will be covered by a dielectric material in the real case. Dielectric materials have low thermal conductivity, and the major heat dissipation path may be through the metallic lines. The overall thermal resistance and heat capacity can vary with the chip design. As confinement of heat is preferred for better switching performance, the expected thermal resistance can also be high in well-designed chips. However, if the chip has lower thermal resistance than the suspended ones we investigated, the temperature rise could drop at a given voltage, and a higher switching voltage amplitude is required. Although our measurement could not fully represent the devices in the real case, the developed model can be used to simulate devices in various environments and help guide the design.

We further demonstrate thermal crosstalk within an array of memristors via heat dissipated by a single device. We constructed a crossbar array of memristors on suspended membranes, identical to the devices studied in this manuscript (in order to enhance thermal isolation and demonstrate thermal crosstalk) [Figs. 4(a) and 4(b)]. We calibrated the response of the system to varying ambient temperatures (500 K and 350 K) [Figs. 4(c) and 4(d)], which exhibits resistance evolution toward a high resistance state, as expected from previous similar measurements.[31] We then measured the temporal change in resistance at different neighboring devices (by fixing the voltage applied to a single device). As expected, these devices exhibited evolution toward a higher resistance due to the temperature rise caused by the operating device. In fact, the magnitude of the evolution is consistent with the distance of the neighboring devices (nearby devices affected the most).

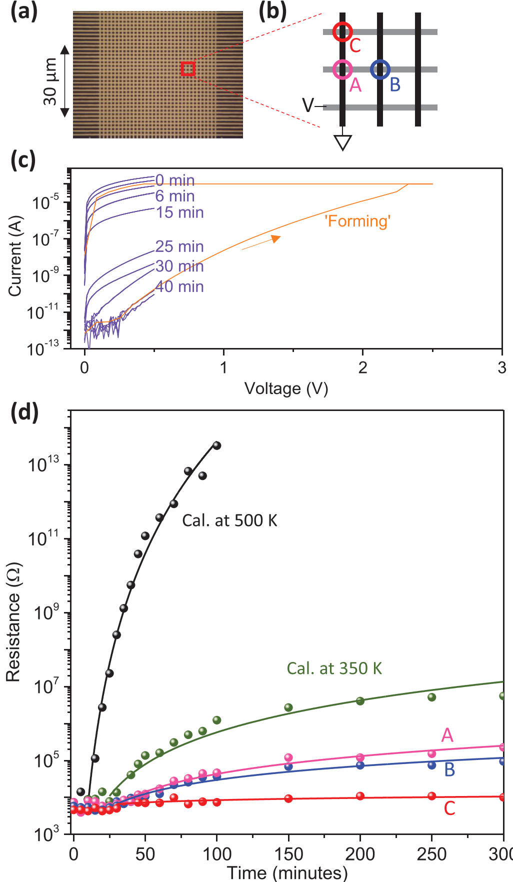

FIG. 4. (a) Optical micrograph of a 32 × 32 crossbar memristor network constructed on a Si_3N_4 membrane, similar to the devices studied in the rest of the manuscript. (b) Schematic of three disturbances studied in three devices ("A"—"C") in response to a single device being driven by electrical stimulus. (c) Calibration of the thermal response of the device being operated by placing the system at an elevated ambient temperature of 500 K. Different low-bias measurements at different time delays (annotated in minutes) are displayed. (d) Evolution of resistance as a function of time, measured at 0.5 V, for two different ambient temperatures (500 K and 350 K), used as calibration curves for modeling. Evolution of resistance as a function of time for the three devices schematically marked in (b), for the operating device held at roughly 1 mA in the steady state. The largest effect on "A" and the smallest effect on "C" are apparent and are expected. Solid data points are experimental data and solid curves are models (color coded to the corresponding experimental data).

Using our model described here and elsewhere,[31] we simulate this effect, which agrees with the experimental data.

In summary, the temperature profile of TaO_x RRAM during operation was measured using an ultrafast imaging system. The maximum temperature rise at the top surface was observed to be ~147 K when a low-resistance-state device was biased at −1.8 V, which was the voltage just before reset, but it is expected that the internal temperature rise can be much higher than the measured temperature for devices with the filament size of only a few nanometers. The active region of measured devices was at the bottom left and around 20% of the device, as indicated by the temperature profile and oxygen

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concentration. A hybrid electro-thermal model comprising 3D heat transfer and 0D resistive switching model was developed. Simulations with the proposed model can explain both I–V and temperature profiles from experiments and can be used for investigating the thermal performance of a system with multiple devices with reasonable computational expense.

See the supplementary material for the I–V curve with DC voltage sweeping, simulated temperature in the direction normal to the device surface, and fitting of thermal resistance and thermal capacitance. Evolution of conductance, temperature, and carrier density is also included in the supplementary material.

DATA AVAILABILITY

The data that support the findings of this study are available within the article and the supplementary material.

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