Theory of Nanocomposite Network Transistors for Macroelectronics Applications

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Abstract

A new class of nanocomposite network materials based on carbon nanotubes or silicon nanowires for thin-film transistors promises significant improvement in the performance of large-area electronics, or macroelectronics. Evaluation of this novel materials technology requires the development of device models. A multicomponent heterogeneous stick-percolation theory is used to show that the key features of this new transistor technology are the consequences of the percolating spatial geometry of the nanosticks (nanotubes, nanorods, or nanowires) that form the channel.

Keywords: *microelectronics, nanoscale, nanostructure.*

Background

Since 2000, there have many reports of a new class of transistors whose channel material is composed of a network of carbon nanotubes (CNTs) or silicon nanowires (SiNWs).[1–12] These nanocomposite network thin-film transistors (NN-TFTs) have numerous potential applications, including high-drive-current microelectronics,[1,2] large-area electronics (macroelectronics),[3–6,11–13] organic electronics,[7,14–16] biochemical sensors,[8–10] and substrate-neutral technologies for heterogeneous integration. This new class of transistors has the potential to reshape the landscape of classical electronics—which has so far been confined to and dominated by single-crystal Si for high-performance, small-footprint microelectronics[17] and by amorphous Si for low-performance macroelectronics[14–16,18]—by introducing a medium-performance (10–100 MHz) technology suitable for large-area fabrication.

In developing a theory of NN-TFTs, one may adopt either a top-down (bulk property)[15,19] or a bottom-up (materials structure) approach.[20,21] The top-down approach assumes that the device obeys square law,[22] according to which the effective mobility fits the theoretical expression for the experimental I–V data. In this approach (particularly for network transistors), the mobility might depend on the geometrical parameters of the device such as channel length L_c and "stick" length (nanotube, nanorod, or nanowire length) L_s. On the other hand, the bottom-up approach considers the system as a network of percolating sticks, where current may not always be inversely proportional to L_c.[23] If the area density of the sticks is below a percolation threshold ($\rho < \rho_c$), no conducting path from source to drain exists, while for $\rho > \rho_c$ the carriers can percolate from stick to stick along one or more paths from source to drain. The bottom-up approach of "stick-percolation,"[24–26] based on percolating electron transport through a collection of nanorod or nanowire "sticks," provides a more powerful theoretical framework for characterizing the properties of NN-TFTs than the top-down approach of effective mobility modeling, which approximates the random media of the sticks with effective homogenized material.

Review of Experimental Results

Experiments on NN-TFTs are characterized by several parameters:

1. The properties (metallic, semiconducting, insulating) of the nanosticks and the encapsulating polymer matrix.
2. The percolating geometry of the network, as characterized by the ratio of L_c to L_s and by the ratio of nanostick area density ρ to the percolation threshold density[27] $\rho_c = 4.236^2/\pi L_s^2$. Here, ρ_c is a critical number per unit area at which a nanostick network starts conducting; 4.236 is a numerical factor with no physical significance. The percolation thresholds for other geometrical shapes (e.g., circular or square) have different values.
3. A processing temperature above or below the plastic melting temperature.

There are four types of NN-TFTs, as summarized in Table I:

- Type I: Short-channel NN-TFTs with $L_c < L_s$,[1,2,28] as in Figure 1a;
- Type II: Long-channel transistors on plastic or silicon substrates with $L_c >> L_s$,[3–6,8–10] as in Figure 1b;
- Type III: Intermediate-channel transistors with aligned sticks,[29] $L_c \sim L_s$; and
- Type IV: Organic TFTs doped with subpercolating metallic nanotubes.[7]

There are significant differences in the processing conditions for the four types of transistors. For example, for TFT applications in flexible macroelectronics (Type II), crystalline CNTs are grown at high temperature on a temporary substrate and then either dispersed in a polymer matrix[12–13] and spin-coated onto a plastic substrate at room temperature, or transferred to a plastic substrate by stamping methods. This creates a co-percolating random network of nearly crystalline semiconducting and metallic nanosticks encapsulated in an insulating polymer matrix. Despite the differences in geometrical structure and processing conditions for the four transistor types, the underlying physics of the transistors turns out to be fundamentally similar.

Generalized Stick-Percolation Model

Since 2004, our group has been developing a generalized stick-percolation model[21,23,28–30] to address the limitations of classical percolation theory, which typically only addresses homogeneous infinite networks. We use instead a heterogeneous, nonlinear, finite-size percolation theory to

unify the description of NN-TFTs, to interpret many counterintuitive features of NN-TFTs, and to highlight fundamental similarities in apparently unconnected experimental results.

Short-Channel Transistors

Type I NN-TFTs ($L_c < L_s$) are short-channel transistors with $L_c < 1$–$2\,\mu m$ based on randomly oriented CNT composites. The stick length is greater than the channel length, so a significant fraction of the tubes directly bridge the source and drain (see Figure 1); the system is therefore always above the percolation threshold, that is, one or more paths connect the source to drain through several sticks.

Since the orientation of the tubes is random, and the probability that a tube will originate at any point is the same, we may conceptually collect all the sticks at one point (preserving the angle with and distance from the channel) to create a "Japanese fan" diagram, as shown in Figures 2a and 2b for two different channel lengths. The number of tubes bridging the channel, N_T, is then given by

$$N_T = \frac{2D_c L_s}{\pi} g(R_s), \tag{1a}$$

where

$$g(R_s) \equiv (\sqrt{1 - R_s^2} - R_s \cos^{-1} R_s)$$

$$\text{and } R_s \equiv \frac{L_c}{L_s}, \tag{1b}$$

and D_c is the (linear) density of CNTs per unit length, of which about two-thirds are semiconducting and one-third are metallic. Once the metallic CNTs are filtered, the same diagram can be used to compute the total current,[22,28]

$$I_D = \zeta(L_c, L_s, D_c, V_D) f(V_G, V_D), \tag{2a}$$

where

$$\zeta \equiv \frac{2D_c}{\pi b^2}\left[bg(R_s) - \cos^{-1} R_s + \frac{2(bR_s + 1)}{\sqrt{b^2 - 1}} \tanh^{-1} \frac{(b-1)\tan(\theta_s/2)}{\sqrt{b^2 - 1}} \right] \tag{2b}$$

and

$$f \equiv \mu_0 L_w C_{ox}[(V_G - V_{TH})V_D - \beta V_D^2], \tag{2c}$$

with $\theta_s = \cos^{-1} R_s$; $b = \lambda / L_c$; and $\lambda = \max(\lambda_B, \lambda_{sat} = V_D \mu_0 / v_{sat})$. In these expressions, V_D is the drain voltage, V_G is the gate voltage, μ_0 is the carrier mobility, V_{TH} is the

Table I: Types of Nanocomposite Network Thin-Film Transistors.

	Type I: SC-CNT ($L_c < L_s$)		Type II-A: NN-CNT ($L_c >> L_s$)		Type II-B: NN-CNT (plastic) ($L_c >> L_s$)		Type II-C: NN-SiNW (plastic) ($L_c > L_s$)		Type III: AL-SiNW ($L_c \sim L_s$)	Type IV: OR-CNT ($L_c >> L_s$)
Material/Percolation Characteristics	S-CNT: $\rho > \rho_c$, random M-CNT: $\rho > \rho_c$, random Matrix: insulating		S-CNT: $\rho > \rho_c$, random M-CNT: $\rho > \rho_c$, random Matrix: insulating		S-CNT: $\rho > \rho_c$, random M-CNT: $\rho > \rho_c$, random Matrix: insulating		S-SiNW: $\rho > \rho_c$, random M-SiNW: N/A Matrix: insulating		S-SiNW: $\rho > \rho_c$, aligned M-SiNW: N/A Matrix: insulating	S-CNT: $\rho \sim \rho_c$, random M-CNT: $\rho < \rho_c$, random Matrix: conducting
Transistor Geometry:										
Channel Length (μm)	0.23		10	2	. . .	100	5		. . .	22
Channel Width (μm)	200		35	200	. . .	250	10		. . .	750
Oxide Thickness (nm)	50		250	100	1500	1700	. . .		. . .	1500
Gate Oxide	Al_2O_3		SiO_2	SiO_2	parylene	resin	epoxy		SiO_2	resin
Substrate	p-Si		Si	Si	polyester	P3HT	plastic		Si	glass/plastic
Performance:										
Mobility, μ (cm^2/V s)	...		10	3–40	0.5–1	0.004	307		~100	0.3
$dI_D/dV_G/V_D$ (A/V²)	0.056		5×10^{-7}	2×10^{-5}	...	...	4×10^{-6}		...	...
Drain Current (μA/μm)	5		...	1	0.040	...	...		...	40–750
Drain Voltage (V)	1		...	5	0.5	...	4		...	100
Applications	microelectronics		TFT/sensor	TFT	sensor	TFT	TFT/sensor		microelectronics	organic electronics
References	1, 2		3, 4	5	8–10	...	6		11	7

SC-CNT: short-channel carbon nanotube; NN-CNT: nanocomposite network carbon nanotube; NN-SiNW: nanocomposite network silicon nanowire; AL-SiNW: aligned silicon nanowire; OR-CNT: carbon nanotube in an organic matrix; L_c: channel length; L_s: "stick" length; S-CNT: semiconducting carbon nanotube; S-SiNW: semiconducting silicon nanowire; M-SiNW: metallic silicon nanowire; M-CNT: metallic carbon nanotube; ρ: percolation area density; ρ_c: percolation threshold density; P3HT: poly(3-hexylthiophene); I_D: drain current; V_G: gate voltage; V_D: drain voltage.

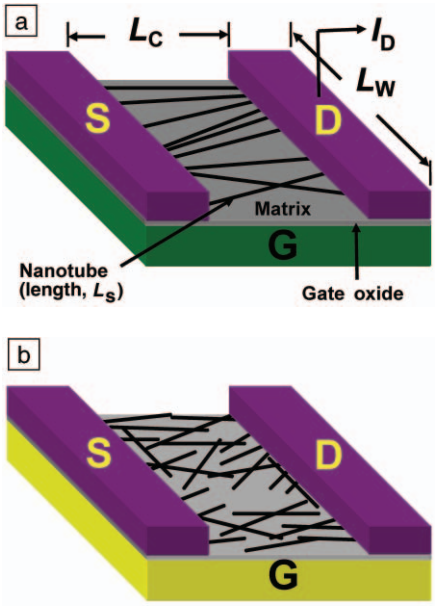

Figure 1. Schematic diagrams for transistors with (a) short channels (nanosticks directly bridge source S and drain D) and (b) long channels (electrons must percolate through the nanostick network to contribute to the drain current). L_c is channel length, L_w is channel width, L_s is stick length; S, D, and G are source, drain, and gate electrodes, respectively.

threshold voltage of the transistor, β is a constant whose value is usually taken as 1/2, λ_B is the mean free path, λ_{sat} is the mean free path for velocity-saturated carriers, and v_{sat} is the saturation velocity of the carriers.

The factorization of I_D into a geometrical component ζ and voltage-dependent component f explains why a short-channel NN-TFT *appears* to behave like a classical field-effect transistor with modified mobility (i.e., $\mu_{eff} = \mu_0 L_s / L_c \zeta$)[21]. Yet, Equation 2 describes a rather complicated microscopic transport phenomena: for a given V_D, the tubes making shallower angles with the channel may be in a linear regime (i.e., $V_D/L_{eff} < E_{crit}$), while the tubes nearly perpendicular to the channel may be in a velocity-saturated regime ($V_D/L_{eff} > E_{crit}$), where L_{eff} is the intercepted channel length of the individual tubes making an angle θ with the channel axis, and E_{crit} is the critical field for velocity saturation. Most significant, Equation 2 captures the fact that the ratio of the numbers of tubes in the linear versus saturation regimes changes as a function of gate and drain biases. Although one can define $\mu_{eff} \sim 1/\zeta$ for compact models, μ_{eff} cannot be interpreted as classical mobility. Classical mobility is independent of L_c, yet μ_{eff} depends on L_c simply because fewer sticks can bridge a longer channel. In other words, the current in a longer-channel transistor is smaller not only because there is backscattering of electrons, but also because there are fewer sticks to carry current. Finally, Equation 2 indicates that the fluctuation in current due to statistical variation in tube number can be reduced if $L_s > 2L_c^{max}$, the maximum channel length. Since L_s is easily controlled during crystal growth, uniform device characteristics are ensured. This device-level homogeneity has significant advantages for the design of macroelectronic integrated circuits.[15–18]

As an example of why μ_{eff} cannot be viewed as classical mobility, consider the burn-in data for CNT SC-TFTs, as shown in Figures 2c and 2d. The metallic tubes that short-circuit the channel must be removed (burned) so that the transistor can be turned on and off with gate voltage. To do so, the semiconducting tubes are first turned off with positive V_G, and then a large drain bias (V_B) is used to burn (by Joule heating or by electromigration) the metallic tubes.[1,2,31] As a fraction α of the metallic tubes burns, the total current drops as $I_D(\alpha) = I_{semi} + [1-\alpha(V_B)]I_M$, as expected, where I_{semi} and I_M are currents in semiconducting and metallic CNTs, respectively. This reduction in I_D is greater in shorter-channel transistors than in longer-channel devices. The "fan diagram" offers a simple interpretation. Initially, the shorter-channel

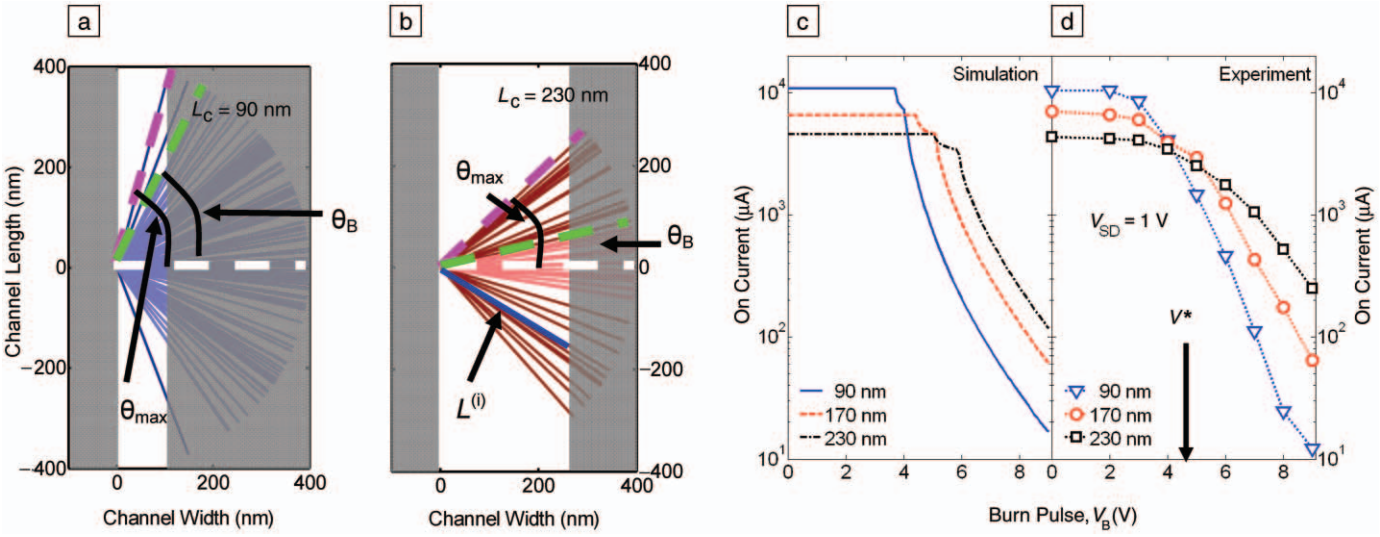

Figure 2. Fan-diagram analysis technique applied to two short-channel nanocomposite network thin-film transistors. Here, stick length is L_s = 400 nm and channel lengths are (a) L_c = 90 nm and (b) L_c = 230 nm. If all sticks in Figure 1a were collected at a point (with angles preserved), it is easy to see that more sticks connect the S/D for a transistor with a shorter channel length before the electrical burning process (dark plus light colored sticks, pink boundary). On the other hand, fewer sticks survive the electrical burning process (dark colored sticks only) for a transistor with a shorter channel length. Here, the burn pulse voltage is such that all the sticks with intercepted channel length $L_i < L_B$ = 235 nm are burned (light-colored sticks, green boundary). (c) The use of numerical simulation to explain current reversal in (d) experimental data. V represents the voltage at which the current reversal happens, and V_{SD} is the source–drain voltage.*

devices have wider-angled fans (compare Figures 2a and 2b). More tubes bridge the channel, so the on-current is larger. However, since the burn current I_B is constant, any given V_B removes all sticks with intercepted channel length $L_{eff} < kV_B/I_B$, where k is a proportionality constant. A given L_{eff} sweeps a larger angle in shorter-channel devices; therefore, a disproportionately larger fraction of bridging tubes are burned in these transistors at any given V_B (the shaded regions in Figures 2a and 2b), and the shorter-channel current drops below the longer-channel current.

Long-Channel Transistors

Type II NN-TFTs ($L_c > L_s$) involve a network (matrix) of nanosticks embedded in insulating polymer (see Figure 1b). The sticks are shorter than the channel so that individual tubes cannot bridge the channel by themselves. Electrons must transfer from one tube to the next at the point of contact between two sticks and eventually percolate down the channel. Three cases are examined in the following.

Channel-Length Scaling: V_G = constant $> V_{TH}$, and V_D is small. We now explore the dependence of I_D on channel length in order to separate the contact effect from bulk effects. We model the TFT channel region by germinating nanosticks at random locations and at random angles. The density of sticks is specified *a priori* and dictates the probability of germination of tubes at any given point. The current through the network is then calculated as follows. In the linear response regime, $V_G > V_{TH}$ and $V_D \sim 0$, the electron density induced in the tubes depends on V_G alone and is spatially invariant. Therefore, diffusion in the network is negligible, and the drift current is given by $J = qn\mu(d\phi/ds)$, where q is electronic charge, n is electron concentration per unit volume, and s defines the distance along individual tubes. Together with the requirement of current continuity at noncontacting points, $dJ/ds \sim 0$, we find $qn\mu d^2(\phi)/ds^2 = 0$. For the intersection points of the ith and jth tubes, $dJ/ds \sim (\phi_i - \phi_j)$, and the continuity equation is generalized to

$$\frac{d^2\phi}{ds^2} + c_{ij}(\phi_i - \phi_i) = 0, \qquad (3)$$

where $c_{ij} = G_m/G_s$,[23,32] the ratio of mutual (G_m) to self-conductances (G_s) at the point of contact. This equation is solved for all the sticks in the network. I_D is obtained by summing the fluxes through all sticks terminating in source or drain contacts. The statistical average of hundreds of such samples for each channel length is shown in Figure 3.

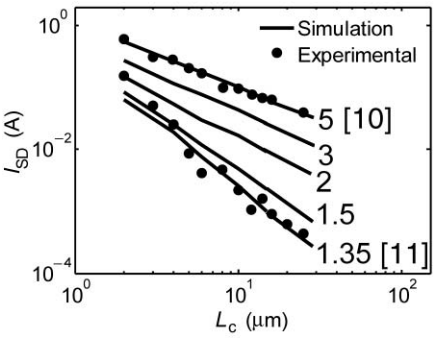

Figure 3. Comparison of percolation model with measured data[3] for the dependence of conductivity with channel length. The number after each curve corresponds to the area density ρ of sticks (μm^{-2}), and the number in square brackets represents the measured density. L_c is channel length and I_{SD} is source–drain current.

Figure 3 shows that the percolation model reproduces experimental data well. The densities estimated from simulation are reasonably close to the experiments. A striking feature of the scaling $\sigma \sim L_c^{-m}$ is the gradual increase in m with reduction in stick density ρ. Phenomenological models based on μ_{eff} would not anticipate such a change in m. However, our percolation approach provides an intuitive explanation: at densities $\rho \sim \rho_c$ and for long-channel-length devices, there are many islands of sticks that remain disconnected from the source/drain and cannot carry current. However, as L_c reduces, the lengths of the existing percolating islands scale with L_c, so that $\sigma \sim 1/L_c$. In addition, previously isolated islands now begin to bridge the channel, *effectively increasing the width*, that is, $W \sim 1/L_c^{(m-1)}$. Therefore, $\sigma \sim W/L_c \sim L_c^{-m}$ with $1 < m < 2$. Therefore, the superlinear scaling of conductivity with channel length reflects the percolation geometry of long-channel NN-TFTs. Finally, the good agreement between theory and experiment for I_D versus L_c solely based on film properties indicates that the contact resistance is negligible and does not dictate device characteristics.

Linear Response: $-V_{TH} < -V_G < -V_{DD}$, $-V_D \sim$ small; here, V_{DD} denotes the voltage of the power supply. The next step is to analyze the quality of the interface between the gate insulator and the channel to ensure that the channel can be turned on and off with relatively low V_G. This would reduce power dissipation as well as hysteresis associated with trapped charges. A key TFT characteristic reported by many groups is the relatively high subthreshold slope, $S = dV_G/d(\log I_D) \sim 1000$ mV/decade ($>> S_{ideal} \sim 100$ mV/dec), as shown in Figure 4. A simple analysis using the Poisson equation[30,33,34] indicates a relatively immature oxide/film interface with a large number of interface traps (~10^7 cm^{-1}) caused perhaps by liquid-based processing. Clearly, N_T must be reduced below 10^4–10^5 cm^{-1} to lower V_{DD} as well as power dissipation. An analysis of the linear response characteristics in Figure 4 also provides a simple interpretation of the transition point at which the on–off ratio reduces abruptly as a function of density. Approximately one-third of the as-deposited CNTs are metallic ($f_M \sim 1/3$). Once metallic tubes reach their own percolation threshold $\rho > \rho_{TH}/f_M$, they provide a direct conducting path between the source and drain that cannot be turned off by gate voltage, leading to a poor on–off ratio, as shown by the top three curves of Figure 4. A self-consistent solution of the Poisson equation and Equation 3 may be used to interpret experimental data[30] and establish that the reduction in N_T should be the key focus for the optimization of NN-TFTs. Recent experiments based on nano-dielectrics as well as substrates grown by atomic layer deposition (ALD) demonstrate that this goal is achievable.[35]

Nonlinear Response: $-V_G < -V_{DD}$, $-V_D < -V_{DD}$. The ultimate frequency response for NN-TFTs for macroelectronics can be determined only if I_D is known at $V_D = V_G = V_{DD}$. Significant hysteresis at large V_D currently precludes easy experimental analysis, but the percolation theory allows simple estimates. The induced carrier concentrations are computed from

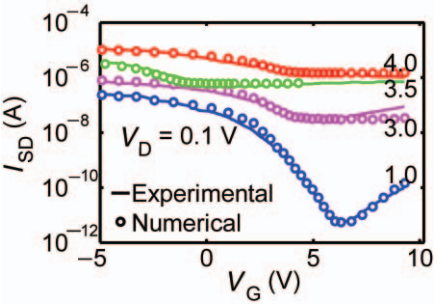

Figure 4. Measured linear response characteristics compared with the percolation model. Low subthreshold slope for the lowermost curve indicates significant interface trap density. The densities ρ = 1, 3, 3.5, and 4 sticks/μm^2 labeling the curves were measured (lowest curve) or simulated (top three curves). I_{SD} is source–drain current; V_G and V_D are gate and drain voltage, respectively.

the transport equation (Equation 3) as a function of V_G and V_D and are solved self-consistently with an approximate 3D Poisson equation, obtained by decoupling the 3D problem into transverse and longitudinal directions.[36] We find that $I_D \sim \zeta f$ (as in Equation 2), even in the nonlinear regime,[20] and that sub-2-μm technology can reach several hundred megahertz if N_T is reduced to acceptable levels.

Aligned Tube Transistors

Type III NN-TFTs ($L_c \sim L_s$) align the nanotubes (see Figure 5)[29] along the channel such that intertube resistive transfer (c_{ij} in Equation 3) is reduced or eliminated. Optimal alignment requires careful consideration. Aligned tubes require fewer interconnections to bridge the channel and improve mobility, but the percolation threshold for aligned tubes increases with orientation anisotropy.[37]

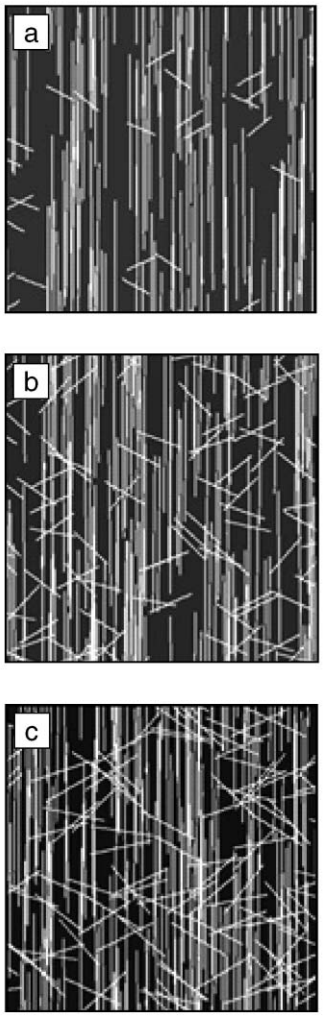

Figure 5. (a)–(c) Samples of randomly generated nanocomposite networks, with increasing density and decreasing alignment of nanosticks. The width of each image is 10 μm.

Sub-Percolating Organic Transistors

Type IV NN-TFTs involve organics embedded with sub-percolating metallic tubes as the channel material. The effective L_c of the composite is reduced because now only the organic links between the metallic sticks must be turned on and off to control transistor performance. Our analysis shows[20] that organic TFT characteristics are predictable consequences of the heterogeneous multicomponent percolation model.

Conclusions

No theoretical foundation for nanocomposite network thin-film transistors comparable with Shockley's theory of classical transistors currently exists. We find that a "bottom-up" approach based on heterogeneous percolation is an effective theoretical framework to classify measured data and to interpret experiments. Our work shows that once tube density, matrix properties, and channel geometry are accounted for, NN-TFT performance data reported in the literature are predictable consequences of our percolation model.

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