Current–Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective

N. Pimparkar, Q. Cao, S. Kumar, J. Y. Murthy, J. Rogers, and M. A. Alam

***Abstract*—By generalizing the classical linear response theory of "stick" percolation to nonlinear regime, we find that the drain–current of a nanobundle thin-film transistor (NB-TFT) is described under a rather general set of conditions by a universal scaling formula $I_D = A/L_S \xi(L_S/L_C, \rho_S L_S^2) \times f(V_G, V_D)$, where A is a technology-specific constant, ξ is a function of geometrical factors such as stick length L_S, channel length L_C, and stick density ρ_S, and f is a function of drain V_D and gate V_G biasing conditions. This scaling formula implies that the measurement of the full current–voltage characteristics of a "single" NB-TFT is sufficient to predict the performance characteristics of any other transistor with arbitrary geometrical parameters and biasing conditions.**

***Index Terms*—Carbon nanotube (NT), inhomogeneous percolation theory, network transistor, thin-film transistor (TFT).**

I. Introduction

OVER the last several years, many research groups have developed nanobundle thin-film transistors (NB-TFTs) based on a percolating network of randomly oriented finite-length silicon nanowires (NWs) and carbon nanotubes (NTs), as shown in Fig. 1. Potential applications include macroelectronics systems such as displays, e-paper, e-clothing, biological and chemical sensors, conformal radar, solar cells, and others [1]–[4]. These applications often require higher performance than amorphous silicon and organics and lower temperature processing than single-crystal Si and poly-Si for flexible substrates such as plastics. Therefore, NB-TFTs based on NW/NTs are expected to be better suited for these high-performance macroelectronic applications.

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N. Pimparkar and M. A. Alam are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-1285 USA.

Q. Cao is with the Department of Chemistry, Beckman Institute, Frederick and Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

S. Kumar and J. Y. Murthy are with the School of Mechanical Engineering, Purdue University, West Lafayette, IN 47907-1285 USA.

J. Rogers is with the Department of Materials Science and Engineering, Chemistry, Electrical and Computer Engineering, Beckman Institute, Frederick and Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

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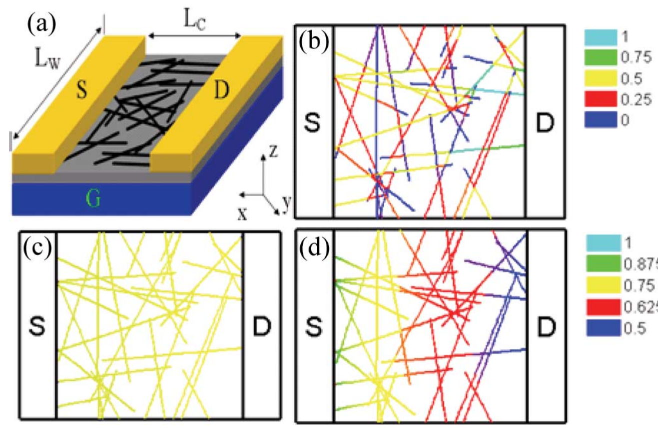

Fig. 1. (a) Schematic of NBT: Geometry of a nanobundle network transistor. (b) Normalized current distribution, which is invariant under any biasing conditions. Normalized conductance distribution along the sticks in the random network in (c) low and (d) high bias. The conductance is uniform along the channel in low bias, while it varies nonlinearly in the high-bias condition, resulting in an inhomogeneous percolating network; the contours of conductance are not straight lines parallel to S/D as in a conventional MOSFET.

The carrier transport characteristics in NB-TFTs (Fig. 1) has been previously modeled and compared to experiments in the linear response regime ($V_{\mathrm{TH}} < V_G < V_{\mathrm{DD}}$, $V_D \sim$ small) (where V_G, V_D, V_{TH}, and V_{DD} are the gate bias, the drain bias, the threshold voltage, and the power supply voltage to the transistor, respectively) [5]. Instead of using a traditional "top-down" phenomenological effective mobility model to describe carrier transport [6], Kumar *et al.* [5] uses a "bottom-up" approach where the properties of the thin film reflects the percolating geometry of NW/NT network. Specifically, in the linear response regime, the charge density induced in each NW/NT, i.e., $n = C_{\mathrm{OX}}(V_G – V_{\mathrm{TH}})$, is a constant independent of V_D. Therefore, the transport properties of NB-TFT in the linear response regime are readily described by the theory of 2-D homogeneous (constant conductivity) stick percolating networks.

The performance limit of NB-TFTs, however, is dictated by the transistor characteristics at high-bias (nonlinear) regime ($V_{\mathrm{TH}} < V_G$, and $V_D < V_{\mathrm{DD}}$). The high interface trap density N_{IT} [7] and large hysteresis associated with current generation of NB-TFTs make stable measurement of their high-bias characteristics difficult. Therefore, a predictive simulation of high-bias operation can be used to establish both the performance limits of NB-TFTs and the relative importance of various device parameters. The fundamental issue is this: Although the spatial geometry of the NW/NT network does not change with bias, the "low-bias" assumption of constant conductivity and local homogeneity along the channel is no longer valid at a "high-bias" regime [see Fig. 1(b) versus Fig. 1(c)]. Since the traditional percolation theory demands global spatial homogeneity, the classical theory cannot be used to analyze the high-bias regime for NB-TFTs.

In this letter, we generalize the classical percolation theory to a nonlinear (high-bias) regime and establish the performance limits for NB-TFTs using a self-consistent solution of drift-diffusion (DD) and Poisson equations. Surprisingly, we find that the conductance exponent $m(I_D \sim 1/L_C^m)$ in the high-bias inhomogeneous case is "exactly" the same as that in the low-bias homogeneous condition [5]. This universal scaling theory implies that the measurement of the full current–voltage $(I–V)$ characteristics of a single transistor can be used to predict the high-bias transistor characteristics of any other NB-TFTs with arbitrary geometrical parameters (e.g., channel length, stick length, etc.) and operating conditions. Previously, we have established the theoretical basis of the scaling formula for short-channel NB-TFTs with $L_C < L_S$ in [8]. In the next section, we show numerically that the scaling formulation holds even for technologically relevant long-channel NB-TFTs with $L_C > L_S$.

II. Computation Model

Fig. 1(a) shows typical NB-TFTs assembled with a bundle of NW/NT of length L_S, which is isotropically oriented $(0 \leq \theta < 2\pi)$ onto the surface of the gate oxide. The probability of germination of NW/NT at each location is dictated by the average density of tubes ρ_s. For NBTs with $L_C > L_S$, the stick–stick interaction is important, and an analytical solution is not possible. The low-bias assumptions [5] that charge density n is constant along the channel and is independent of V_D do not apply at high-bias conditions. Therefore, $n(V_D, V_G)$ must be determined self-consistently by solving the DD equations (appropriate for $L_C > 1\ \mu$m) and the Poisson equation. In the bottom-up description of the channel, the DD–Poisson equations are generalized for NB-TFTs as

$$\left.\begin{array}{c}\frac{d^2\Phi}{dV^2}+\frac{\rho}{\varepsilon}=0\\ \nabla\cdot J_p=0\\ \nabla\cdot J_n=0\end{array}\right\}\rightarrow$$

$$\begin{aligned}\sum_{i=1}^{N}\left(\frac{d^2\Phi_i}{ds^2}+\frac{\rho_i}{\varepsilon}-\frac{(\Phi_i-V_G)}{\lambda^2}+\sum_{j\neq i}\frac{(\Phi_j-\Phi_i)}{\lambda_{ij}^2}\right)&=0\\ \sum_i\left(\nabla\cdot J_{pi}+\sum_{j\neq i}C_{ij}^p(p_j-p_i)\right)&=0 \qquad (1)\\ \sum_i\left(\nabla\cdot J_{ni}+\sum_{j\neq i}C_{ij}^n(n_j-n_i)\right)&=0\end{aligned}$$

where N is the total number of NT/NWs (assumed undoped $N_A = 0$, i.e., the initial Fermi level is equal to the intrinsic level or $E_F = E_i$), s is in the direction of individual NW/NT, ρ is the total charge density, and the term $-(\Phi - V_G)/\lambda^2$ (the well-known parabolic approximation [9], [10]) introduces the effect of back gate, where λ is the effective screening length with $\lambda^2 = \varepsilon_{\mathrm{NT}} T_{\mathrm{ox}} d/\varepsilon_{\mathrm{OX}}$. For typical transistor parameters, $d \sim$ 2 nm is the thickness of the nanobundle film, $T_{\mathrm{ox}} \sim 250$ nm is the thickness of the gate oxide, $\varepsilon_{\mathrm{NT}} \sim 5$ [11] and $\varepsilon_{\mathrm{OX}} \sim 3.9$ are the dielectric constants for the NT network and gate oxide, respectively, which give $\lambda \sim 44$ nm. The parabolic approximation is valid in this case because the condition that $L_C \gg \lambda \gg d$ is satisfied. The term $(\Phi_j–\Phi_i)/\lambda_{ij}^2$ is the stick–stick interaction with screening length λ_{ij}, where a node on stick i intersects a node on stick j. The intersecting nodes act as tiny gates for each other, modifying the potential and carrier concentrations [12]. Furthermore, transport is essentially 1-D (along the tube), with the additional term $C_{ij}^n(n_j - n_i)$ in the continuity equation representing the charge transfer between the nanosticks at the point of intersection. Here, a higher value of $C_{ij}^{n,p} = G_0/G_1$ implies better electrical contact, where G_0 and G_1 are the mutual and self-conductances of the tubes. We assume that $C_{ij} = 50$ [5] and $\lambda_{ij} = 1$ nm for a well-contacted network.

III. Results and Discussion

It was shown in [8] that in the "short-channel" limit of $L_C < L_S$ and at low stick density, the NW/NTs behave as individual transistors connected in parallel; therefore, the ratio of I_D for any two bias points is independent of the geometry of the NB-TFTs. This implies that the scaling relationship is (assuming that contact resistance R_S is negligible or has been subtracted out)

$$I_D = \frac{A}{L_S}\xi\left(\frac{L_S}{L_C}, \rho_s L_S^2\right) \times f(V_G, V_D) \qquad (2)$$

where the proportionally constant A depends on oxide capacitance C_{OX}, tube diameter d [13], and stick–stick interaction parameter $C_{ij}^{n,p}$. In addition, ξ and f are functions of geometrical parameters (L_S, L_C, and ρ_S) and bias conditions (V_D and V_G), respectively. The factorization is consistent with the experimental data, as shown in [8, Fig. 10].

For long-channel NB-TFTs with $L_C > L_S$ [see Fig. 1(a)], the individual sticks cannot bridge the channel by themselves, and stick–stick interaction becomes important $(C_{ij}^{n,p} \neq 0)$. Fig. 2 summarizes the self-consistent solution of (1) for different bias conditions [Fig. 2(a)] and various geometrical parameters [Fig. 2(b) and (c)] for long-channel NB-TFTs. Each point of Fig. 2 reflects the average solution of $\sim$200 statistical samples, and generation of Fig. 2 requires approximately 15 h on 200 nodes of a cluster with 3.2 GHz and 64-bit Intel Irwindale processors with 4 GB of memory. We performed experiments [14], [15] to check the current scaling, and remarkably, the experimental data support our results very well, as shown in Fig. 2(b) and (c) for low and high bias, respectively. These results indicate that the scaling formula (2) holds for arbitrary geometrical and biasing conditions even in the

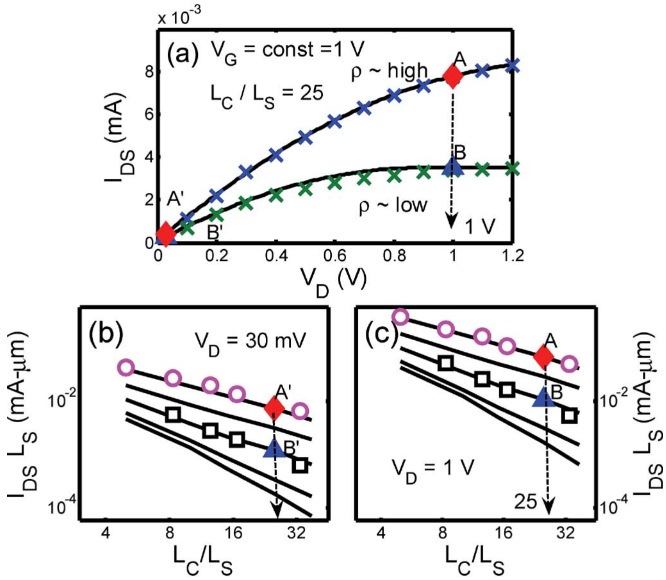

Fig. 2. (a) Simulations (curves) and experimental data ("x") for the I_D–V_D of two different random networks with high and low density, respectively. A, A' (solid diamond) and B, B' (solid triangle) represent points on the plot corresponding to high and low V_D, respectively. (b) and (c) Drain–current versus channel length for network transistors, with channel length $L_C >$ stick length and $L_S \sim 6\ \mu$m for low and high bias, respectively, in strong coupling limits. Different curves correspond to density $\rho_S L_S^2 = 5.4$, 6, 8, 12, and 20 and $m = 1.9$, 1.7, 1.4, 1.2, and 1.07, respectively. The experimental data for high density (open circles) and low density (open squares) are also shown. The absolute values of the experimental results are scaled since they were performed on two different devices. The current exponents m for the high-bias regime are *exactly* the same as those for the low-bias regime, and (2) requires for any particular percolating random network that $I_A/I_{A'} = I_B/I_{B'}$.

"long-channel limit" of $C_{ij}^{n,p} \neq 0$. Specifically, (2) requires that for the geometrical scaling factor, $\xi(L_S/L_C, \rho_S L_S^2)$ remains invariant (up to a scaling factor) of biasing conditions, which is easily confirmed by comparing Fig. 2(b) and (c). Indeed, we find that (once the series resistance has been accounted for)

$$\xi\left(\frac{L_S}{L_C}, \rho_s L_S^2\right) = \left(\frac{L_S}{L_C}\right)^{m(\rho_s L_S^2)} \tag{3}$$

where m is a universal exponent of the stick percolating system. For densities much higher than the percolation threshold ($\rho_S L_S^2 \gg \rho_{\mathrm{th}} L_S^2 = 4.236^2/\pi$ [16]), the network behaves as a 2-D conductor with $m = 1$. Together with (4), we find that (2) reduces to the classic "square law" as expected. However, for densities near the percolation threshold ($\rho_S L_S^2 \sim 4.236^2/\pi$), the exponent takes the value $m \sim 1.8$ [Fig. 2(b)]. Moreover, Fig. 2(a) shows that the bias-dependent scaling function

$$f(V_G, V_D) = \left[(V_G - V_{\mathrm{TH}})V_D - \beta V_D^2\right] \tag{4}$$

is independent of geometrical parameters ($\beta \sim 0.5$), again satisfying (2). It is hardly surprising that the voltage scaling function $f(V_G, V_D)$ would follow the classical square-law formula at very low ($\rho \ll \rho_{\mathrm{th}}$, and $L_C < L_S$) and at very high densities ($\rho \gg \rho_{\mathrm{th}}$). After all, for $\rho \ll \rho_{\mathrm{th}}$ and $L_C < L_S$, the stick–stick interaction is negligible, and the sticks bridge the source and drain (S/D) directly; therefore, the system behaves as an independent collection of 1-D (long-channel) conductors, and the conclusions of [8] apply. At $\rho \gg \rho_{\mathrm{th}}$, the percolating network approximates a classical 2-D homogeneous thin film (fractal dimension $D_F > 1.8$ compared to $D_F = 2$ for thin film), and once again, the classical MOSFET formula should hold. "The real surprise and the most significant finding of our analysis is that (2) holds for the arbitrary stick density above and below (with $L_C < L_S$) the percolation threshold."

Our results imply that once V_{TH} and β are determined [for (4)] by I_D–V_D and I_D–V_G measurement and m is determined from Fig. 2(b) for particular L_S, L_C, and ρ_S, one can readily determine the technology-specific constant A. Given A, V_{TH}, and β, we can determine [by (2)] the transistor performance of any other transistor of arbitrary L_S, L_C, and ρ_S [Fig. 2(b)] and biasing condition. This scaling formula could therefore reduce the technology development and characterization time significantly. Second, (2) provides a "bottom-up definition of effective mobility $\mu_{\mathrm{eff}} \sim (dI_D/dV_G/V_D)(L_S/\xi)/(L_W C_{\mathrm{OX}})$," the value of which is independent of L_C and can be used to compare experimental data from various laboratories. For very high density networks, μ_{eff} reduces to a conventional mobility equation as $m = 1$ and $\xi = L_S/L_C$ in (3). Finally, (1) and (2) can be used to compute $f_{\max} = I/CV$ to establish the ultimate performance limits of NB-TFTs free from nonideal factors such as hysteresis or interface traps, which give ~1 GHz of device speed for the NB-TFT in [2] for $L_C = 1\ \mu$m.

IV. Conclusion

We have generalized the linear stick percolation theory to nonlinear regime to find a scaling formula (2) to compute the I_D–V_D characteristics of NB-TFTs that once calibrated, can be used to establish the performance limits of NB-TFTs of arbitrary geometry and operating conditions. Our analysis therefore would help organize experimental data from various research groups and could have significant impact on the development of NB-TFT technology.

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