**Theory of transfer characteristics of nanotube network transistors**

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Carbon nanotubes (CNT) nanocomposites used for thin-film transistors (TFTs) provide one of the first technologically-relevant test beds for two-dimensional heterogeneous percolating systems. The characteristics of these TFTs are predicted by considering the physics of heterogeneous finite-sized networks and interfacial traps at the CNT/gate-oxide interface. Close agreement between our numerical results and different experimental observations demonstrates the capability of the model to predict the characteristics of CNT/nanowire-based TFTs. Such predictive models would simplify device optimization and expedite the development of this nascent TFT technology. © 2006 American Institute of Physics. [DOI: 10.1063/1.2187401]

Thin-film transistors (TFTs) based on two-dimensional (2D) networks of carbon nanotubes (CNTs) or silicon nanowires have recently been explored for low voltage, high-reliability, high-speed (>GHz) applications in flexible macroelectronics1–8 as well as in CNT microelectronics.9,10 Despite their promise to improve the performance of microelectronics and macroelectronics, a number of technical difficulties remain, which include: (i) Poor subthreshold characteristics (800 mV/dec ~ 2500 mV/dec) and (ii) a lack of understanding of on-off current (I_{ON},I_{OFF}) dependence on parameters such as the channel length (L_C), tube length (L_T), and the fraction of metallic tubes [f_M=(N_M)/(N_M+N_3)]. The properties of these 2D CNT networks are controlled by the competition between heterogeneous networks of metallic and semiconducting CNTs, a regime that has never before been explored. A predictive model is required to interpret experimental results and to expedite the development of this new class of TFTs.

In this letter, using a detailed computational model of heterogeneous percolating networks, we show that the high subthreshold slope (S) is a consequence of interface traps (N_{IT}) at the CNT/gate-oxide interface. We also establish that the on/off ratio (R) is a unique and unpredictable function of L_C, L_T, N_{IT}, f_M, and ρ, the tube density, and deduce ρ from R when the other parameters are known. Finally, we calculate the ultimate performance limits of network transistors free from interface traps (N_{IT}→0) and metallic CNT contamination (f_M→0).

We represent the network transistor [see Fig. 1(a)] as a 2D percolating random network of nanotubes of length L_T and diameter d dispersed in a domain of channel length L_C and channel width H. Since L_C≪λ, the mean-free path, we use semiclassical transport theory (Poisson equations augmented by a drift-diffusion model) in our analysis.11,12

The potential at any point in the CNT network is given by 

\[ V_p = \psi_s(V_G) + \psi_i(V_D) \]

where \( \psi_s(V_G) \) is the CNT surface potential due to the gate voltage \( V_G \) and \( \psi_i(V_D) \) is the potential due to the source/drain voltage \( V_D \). Since \( V_G \gg V_D \), \( \psi_s(V_G) \gg \psi_i(V_D) \), the hole (p) and electron (n) concentrations depend on \( V_G \) alone. Therefore, the three-dimensional (3D) Poisson equation \( \nabla^2 V = q(n-p)/\epsilon \) reduces to a 2D problem across the transistor cross section [Fig. 1(b)], i.e.,13,14

![FIG. 1. Color online](image-url) (a) A thin-film network transistor with channel length \( L_C \), channel width \( H \), and individual tube length \( L_T \), source (S), drain (D), and gate (G) are also indicated. (b) X-Y cross section of the TFT transistor in (a) showing field lines for a single tube. (c) Current-voltage (I_{ON} vs. V_D) plots showing the on-current (I_{ON}), defined at \( V_G=0.1 \) V and \( V_D=-15 \) V, and off-current (I_{OFF}), defined at \( V_G=0.1 \) V and \( V_D=0 \) V and subthreshold slope (S ~ 1 V/dec) for a network transistor device. (d) Carrier concentration vs gate voltage for different values of interface trap capacitance for a device with oxide thickness 250 nm (Ref. 6) and oxide capacitance \( C_{OX} = 0.18 \text{ pF/cm} \). The interface trap density corresponding to \( C_{IT} = [0,1.6,2.5,6.4] \text{ pF/cm} \) is \( N_{IT} = [0,1.1,6.4] \times 10^{17} \text{ cm}^{-2} \) at \( \varphi = 1 \text{ V} \), and the subthreshold slope is \( S = [0.06,0.66,1.02,2.46] \text{ V/dec} \), respectively.
where $\alpha_{\text{eq}}=0.142$ nm is the C–C bond length, $t=3$ eV is the C–C bond energy, and $E_g$ is the band gap of the s-SWCNT. The gate voltage is given by $V_{G}=V_{\text{OX}}+\psi_{S}$, where the voltage drop across the gate oxide is $V_{\text{OX}}=\Phi_{\text{MS}}+(Q_{i}+Q_{\text{ox}})/C_{\text{OX}}$. Here, $\Phi_{\text{MS}}$ is the work function difference of the gate metal electrode and the single-wall CNT (SWCNT), $Q_{i}$ and $Q_{\text{ox}}$ are the total charge during inversion and the interface charge, respectively. Although $N_{\text{IT}}$ is negligible for the short-channel single-tube CNT transistors reported in the literature, however, low-temperature processing, longer channel lengths, and multiple tubes, dictate that $N_{\text{IT}}$ be explicitly accounted for network transistors. The gate voltage is

$$V_{G} = \left( \frac{1}{\alpha_{\text{eq}}} + \frac{C_{\text{IT}} + C_{O}}{C_{\text{OX}}} \right) \psi_{S} - q(p-n)/C_{\text{OX}} + V_{\text{FB}},$$

(2)

where $\alpha_{\text{eq}}=C_{\text{eq}}/(C_{\text{OX}}+C_{r}+C_{p})$ is the gate control factor ($\sim 1$ for long channel devices), $C_{\text{OX}}$ is the oxide capacitance, $C_{Q}$ is the quantum capacitance ($\sim 0$ for subthreshold region of CNT field effect transistors), and $C_{\text{IT}}=d(qN_{\text{IT}})/d\psi_{S}$ is the capacitance due to interface charges ($N_{\text{IT}}$). The sub-threshold slope is given by $S=m(2.303kT/q)$ where $m=1+C_{\text{IT}}/C_{\text{OX}}$. Experimentally measuring $S$ allows the calculation of $C_{\text{IT}}$. Once $C_{\text{IT}}$ is determined, Eqs. (1) and (2) can be solved iteratively for the 2D geometry to calculate the hole density $p(V_{G})$ [Fig. 1(d)].

We use semiclassical transport theory to compute device characteristics, accounting for tube-tube contact. The current along the tube is given by $J=q\mu_{s}n(V_{G})d\phi(V_{DS})/ds$. Using the continuity equation $dJ/ds=0$, the dimensionless potential distribution $\phi_{s}$ along tube $i$ is given by,

$$\frac{d^{2}\phi_{i}}{ds^{2}} - c_{ij}(\phi_{i}-\phi_{j}) = 0,$$

(3)

Here, $s$ is the length along the tube (normalized to grid spacing) and $c_{ij}=G_{ij}/G_{1}$ where $G_{ij}$ and $G_{1}$ are the mutual and self-conductance of the tubes, respectively. The quantity $c_{ij}$ is the dimensionless charge-transfer coefficient between tubes $i$ and $j$ at their intersection point and is specified a priori; it is nonzero only at the point of intersection. The problem is solved numerically using the finite volume method. Transport through the insulating gate substrate is assumed to be negligible.

Using the above formulation, we compute $I_{SD}$ versus $V_{G}$ for several tube densities ($p=1-5 \times 10^{12}$ cm$^{-2}$) as shown in Fig. 2. The device parameters $L_{C}=10 \mu$m, $L_{S}=2 \mu$m, $H=35 \mu$m, and $V_{\text{FB}}=0.1$ V are chosen to match the experiments in Ref. 6. Since $L_{F} \gg L_{S}$, these transistors are called long-channel devices. We use $c_{ij}=50$ based on typical values for CNT tube-tube contact, mobility, and density function theory. Here, $f_{M}$, is taken to be $33\%$ in Fig. 2, consistent with Ref 6. The conductance ratio of metallic to semiconducting tubes (M/S conductance ratio) in the on state is chosen as $8.0$, consistent with Ref. 10. In general, the M/S conductance ratio depends weakly on the fabrication process, as well as the chirality, band gap, and the diameter of the tubes.

![FIG. 2. (Color online) Computed $I_{SD}$–$V_{G}$ at $V_{DS}=0.1$ V for different densities is compared with experimental results (from Ref. 6) before the electrical breakdown of metallic tubes. The number after each curve corresponds to tube density $p$. The curve $p=3.5$ $\mu$m$^{-2}$ is shifted on the $x$ axis to account for charge trapping.](image-url)
network transistors can be designed as if they were ordinary transistors using standard design tools. Regarding Question 2, even if the metallic tubes cannot be removed, an excellent on-off ratio is still maintained for long channel transistors if $\rho < \rho_{\text{th}}/f_{\text{M}}$. In addition, if $N_{\text{IT}}$ can be improved by better processing, the gate voltage can be lowered to $3–5$ V, while maintaining the on/off ratio and the drive current.

In summary, a heterogeneous finite-size percolation model has been developed to explore the dependence of gate characteristics in the linear regime on tube density and metallic contamination for thin films made of randomly oriented nanotubes. The on-off ratio before and after the breakdown of metallic tubes is analyzed and explained. The results presented here should be a powerful and unique predictive modeling capability for the analysis, design, and development not only of TFTs but in any two-component system with competing materials, e.g., metal CNT saturated organics and organic photovoltaic applications.26

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