Theory of transfer characteristics of nanotube network transistors

S. Kumar[a)]
Department of Mechanical Engineering, Purdue University, West Lafayette, Indiana 47907-1285

N. Pimparkar
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907-1285

J. Y. Murthy
Department of Mechanical Engineering, Purdue University, West Lafayette, Indiana 47907-1285

M. A. Alam
School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907-1285

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Carbon nanotubes (CNT) nanocomposites used for thin-film transistors (TFTs) provide one of the first technologically-relevant test beds for two-dimensional heterogeneous percolating systems. The characteristics of these TFTs are predicted by considering the physics of heterogeneous finite-sized networks and interfacial traps at the CNT/gate-oxide interface. Close agreement between our numerical results and different experimental observations demonstrates the capability of the model to predict the characteristics of CNT/nanowire-based TFTs. Such predictive models would simplify device optimization and expedite the development of this nascent TFT technology. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2187401]

Thin-film transistors (TFTs) based on two-dimensional (2D) networks of carbon nanotubes (CNTs) or silicon nanowires have recently been explored for low voltage, high-reliability, high-speed (>GHz) applications in flexible macroelectronics[1–8] as well as in CNT microelectronics.[9,10] Despite their promise to improve the performance of microelectronics and macroelectronics, a number of technical difficulties remain, which include: (i) Poor subthreshold characteristics (800 mV/dec ~ 2500 mV/dec) and (ii) a lack of understanding of on-off current (I_{ON}, I_{OFF}) dependence on parameters such as the channel length (L_C), tube length (L_T), and the fraction of metallic tubes [$f_M = N_M/(N_M+N_S)$]. The properties of these 2D CNT networks are controlled by the competition between heterogeneous networks of metallic and semiconducting CNTs, a regime that has never before been explored. A predictive model is required to interpret experimental results and to expedite the development of this new class of TFTs.

In this letter, using a detailed computational model of heterogeneous percolating networks, we show that the high subthreshold slope (S) is a consequence of interface traps (N_{IT}) at the CNT/gate-oxide interface. We also establish that the on/off ratio (R) is a unique and predictable function of L_C, L_T, N_{IT}, f_M, and ρ, the tube density, and deduce ρ from R when the other parameters are known. Finally, we calculate the ultimate performance limits of network transistors free from interface traps ($N_{IT} \to 0$) and metallic CNT contamination ($f_M \to 0$).

We represent the network transistor [see Fig. 1(a)] as a 2D percolating random network of nanotubes of length L_T and diameter d dispersed in a domain of channel length L_C and channel width H. Since $L_C \gg \lambda$, the mean-free path, we use semiclassical transport theory (Poisson equations augmented by a drift-diffusion model) in our analysis.[11,12]

The potential at any point in the CNT network is given by $V_{i,s} = \psi_S(V_G) + \phi_i(V_{DS})$, where $\psi_S(V_G)$ is the CNT surface potential due to the gate voltage V_G and $\phi_i(V_{DS})$ is the potential due to the source/drain voltage V_{DS}. Since $V_G \gg V_{DS}$, $\psi_S(V_G) \gg \phi_i(V_{DS})$, the hole ($p$) and electron ($n$) concentrations depend on V_G alone. Therefore, the three-dimensional (3D) Poisson equation $\nabla^2 V = q(n-p)/\varepsilon$ reduces to a 2D problem across the transistor cross section [Fig. 1(b)], i.e.,[13,14]

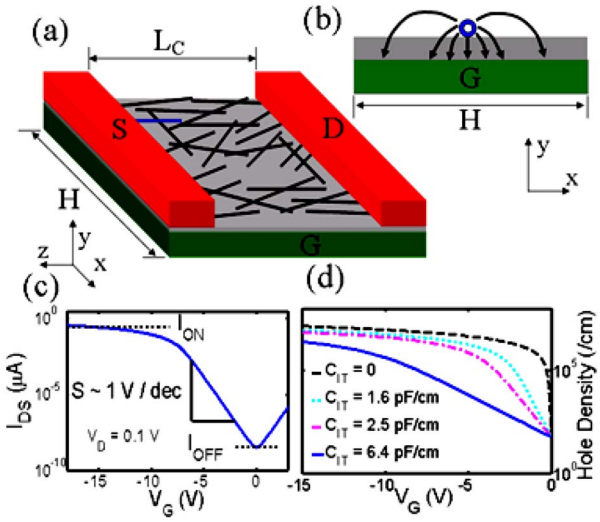

FIG. 1. (Color online) (a) A thin-film network transistor with channel length L_C, channel width H, and individual tube length L_S. Source (S), drain (D), and gate (G) are also indicated. (b) X-Y cross section of the TFT transistor in (a) showing field lines for a single tube. (c) Current-voltage (I_{DS}-V_G) plots showing the on-current (I_{ON}, defined at $V_D = 0.1$ V and $V_G = -15$ V) and off-current (I_{OFF}, defined at $V_D = 0.1$ V and $V_G = 0$ V) and subthreshold slope ($S \sim 1$ V/dec) for a network transistor device. (d) Carrier concentration vs gate voltage for different values of interface trap capacitance for a device with oxide thickness 250 nm (Ref. 6) and oxide capacitance $C_{OX} = 0.18$ pF/cm. The interface trap density corresponding to $C_{IT} = [0, 1.6, 2.5, 6.4]$ pF/cm is $N_{IT} = [0, 1, 1.6, 4] \times 10^7$/cm at $\varphi_s = 1$ V, and the subthreshold slope is $S = [0.06\ 0.66\ 1.02\ 2.46]$ V/dec, respectively.

a)Electronic mail: kumar21@purdue.edu

$$p,n = \frac{8}{3\pi a_{cc} t}\int_{-\infty,E_C}^{E_V,\infty} \frac{E}{\sqrt{E^2-(E_G/2)^2}} \frac{dE}{1+\exp\left(\frac{E \pm q\psi_S}{k_B T}\right)}, \tag{1}$$

where $a_{cc}=0.142$ nm is the C–C bond length, $t=3$ eV is the C–C bond energy, and E_G is the band gap of the s-SWCNT. The gate voltage is given by $V_G=V_{\rm OX}+\psi_S$, where the voltage drop across the gate oxide is $V_{\rm OX}=\Phi_{MS}+(Q_i+Q_{\rm it})/C_{\rm OX}$. Here, Φ_{MS} is the work function difference of the gate metal electrode and the single-wall CNT (SWCNT), Q_i and $Q_{\rm it}$ are the total charge during inversion and the interface charge, respectively. Although $N_{\rm IT}$ is negligible for the short-channel single-tube CNT transistors reported in the literature,[13] however, low-temperature processing, longer channel lengths, and multiple tubes, dictate that $N_{\rm IT}$ be explicitly accounted for network transistors. The gate voltage is

$$V_G = \left(\frac{1}{\alpha_G}+\frac{C_{\rm IT}+C_Q}{C_{\rm OX}}\right)\psi_S - q(p-n)/C_{\rm ox} + V_{\rm FB}, \tag{2}$$

where $\alpha_G=C_{\rm ox}/(C_{\rm ox}+C_S+C_D)$ is the gate control factor (~ 1 for long channel devices), $C_{\rm OX}$ is the gate oxide capacitance, C_Q is the quantum capacitance (~ 0 for subthreshold region of CNT field effect transistors),[14] and $C_{\rm IT}=d(qN_{\rm IT})/d\psi_S$ is the capacitance due to interface charges ($N_{\rm IT}$). The subthreshold slope is given by $S=m(2.303kT/q)$ where $m=1+C_{\rm IT}/C_{\rm OX}$. Experimentally measuring S allows the calculation of $C_{\rm IT}$. Once $C_{\rm IT}$ is determined, Eqs. (1) and (2) can be solved iteratively for the 2D geometry to calculate the hole density $p(V_G)$ [Fig. 1(d)].

We use semiclassical transport theory to compute device characteristics, accounting for tube-tube contact.[11,15–21] The current along the tube is given by $J=q\mu n(V_G)d\phi(V_{DS})/ds$. Using the continuity equation $dJ/ds=0$, the dimensionless potential distribution ϕ_i along tube i is given by,[11]

$$\frac{d^2\phi_i}{ds^2} - c_{ij}(\phi_i-\phi_j)=0. \tag{3}$$

Here, s is the length along the tube (normalized to grid spacing) and $c_{ij}=G_0/G_1$ where G_0 and G_1 are the mutual and self-conductance of the tubes, respectively. The quantity c_{ij} is the dimensionless charge-transfer coefficient between tubes i and j at their intersection point and is specified *a priori*; it is nonzero only at the point of intersection. The problem is solved numerically using the finite volume method.[11,22] Transport through the insulating gate substrate is assumed to be negligible.

Using the above formulation, we compute I_{SD} versus V_G for several tube densities ($\rho=1-5$ μm^{-2}) as shown in Fig. 2. The device parameters $L_C=10$ μm, $L_S=2$ μm, $H=35$ μm, and $V_D=0.1$ V are chosen to match the experiments in Ref. 6. Since $L_C \gg L_S$, these transistors are called long-channel devices. We use $c_{ij}\sim 50$ based on typical values for CNT tube-tube contact,[6,11,19] mobility,[6] and density function theory.[23] Here, f_M, is taken to be 33% in Fig. 2, consistent with Ref 6. The conductance ratio of metallic to semiconducting tubes (M/S conductance ratio) in the on state is chosen as 8.0, consistent with Ref. 10. In general, the M/S conductance ratio depends weakly on the fabrication process, as well as the chirality, band gap, and the diameter of the tubes.

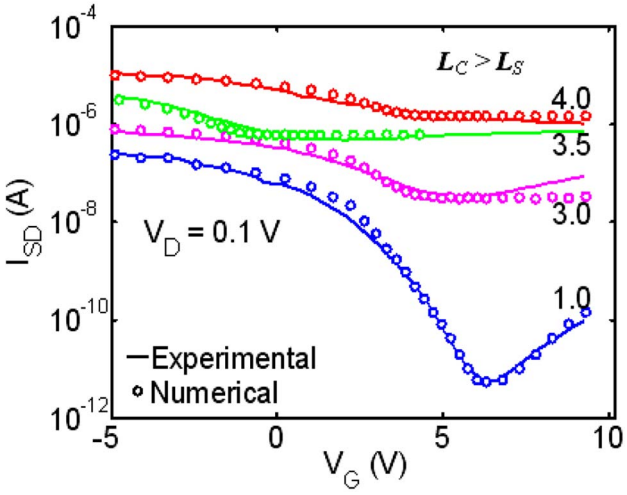

FIG. 2. (Color online) Computed $I_{SD}\sim V_G$ at $V_D=0.1$ V for different densities is compared with experimental results (from Ref. 6) before the electrical breakdown of metallic tubes. The number after each curve corresponds to tube density ρ. The curve $\rho=3.5$ μm^{-2} is shifted on the x axis to account for charge trapping.

To interpret the on/off current ratio observed in Ref. 6, note that $S\sim 1$ V/dec at $\rho=1$ μm^{-2} [Fig. 1(c)] corresponds to $m\sim 16$. By solving Eqs. (1) and (2) self-consistently, we find $C_{\rm OX}\sim 0.18$ pF/cm (Ref. 13) and $C_{\rm IT}=2.72$ pF/cm (or $N_{\rm IT}=C_{\rm IT}/q=1.8\times 10^7\times\psi_S$ cm^{-1}). This is approximately 0.5% of the density of carbon atoms ($\sim 3\times 10^9$ cm^{-1} for a SWCNT of diameter 2 nm) for $\psi_S=1$ V. Gate characteristics are computed by solving Eqs. (2) and (3) for a specific network configuration. An average is then taken over 50 random realizations of the network. Computations for $\rho=1$ μm^{-2} agree very well with experiments in Ref. 6, Fig2. Increasing ρ increases the number of percolating metallic paths, increasing $I_{\rm ON}$, but reducing R, as in Ref. 6. Reference 6 *speculates* that $\rho>3$ μm^{-2} for devices with low on-off ratio (top three solid lines in Fig. 2 of Ref. 6). *Our simulations establish that they correspond to exact densities of* $\rho=3.0$, 3.5, *and* 4.0, *respectively. Thus, tube density* ρ *may be deduced from a simple electrical measurement of the on/off current ratio* (see Fig. 2 herein) *obviating the need for inaccurate and time-consuming analysis of atomic force microscopy (AFM) images*. We note, however, that although we can predict $R(\rho)$ for a fixed M/S conductance ratio and c_{ij}, the absolute value of the on-off current and R can still vary from sample to sample depending on the M/S conductance ratio and the contact conductance between tubes of different diameters. The same methodology and a similar set of parameters can also be used to interpret the short channel data from John Roger's group (Fig. 2 in Ref. 7) and this demonstrates the predictive power of the theoretical framework. Details of the analysis for short channel-length devices will be published elsewhere.

The developed model allows us to answer two questions of fundamental technological importance: (1) What are the performance limits of network transistors free from metallic tubes ($f_M=0$)?, and (2) given a technology-specific f_M, what is the maximum density of tubes (ρ_{max}) that will preserve a high on-off ratio? To answer the first question, we see in Fig. 3 that the maximum achievable on-off ratio is $\sim 5\times 10^4$ after the removal of metallic paths, and this ratio is nearly independent of ρ for $\rho \gg \rho_{\rm th}$ $(=4.23^2/\pi L_S^2)$.[8,24] The on-current, however, rises superlinearly for $\rho > 2-3\rho_{\rm th}$. Beyond this den-

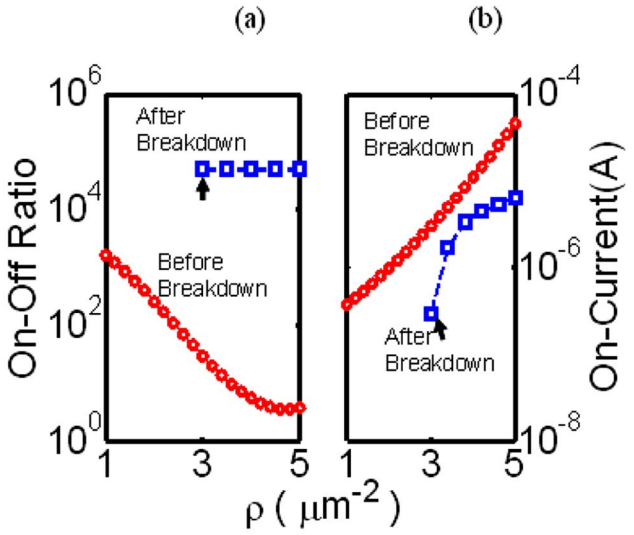

FIG. 3. (Color online) Dependence of (a) On-off ratio and (b) On-current on network density before and after the removal of metallic tubes. L_S=10 μm, L_C=2 μm, and H=35 μm. The network drops below the percolation limit after breakdown for the tube density indicated by arrows.

sity, network transistors can be designed as if they were ordinary transistors using standard design tools. Regarding Question 2, even if the metallic tubes cannot be removed, an excellent on-off ratio is still maintained for long channel transistors if $\rho < \rho_{\text{th}}/f_M$. In addition, if N_{IT} can be improved by better processing, the gate voltage can be lowered to 3–5 V, while maintaining the on/off ratio and the drive current.

In summary, a heterogeneous finite-size percolation model has been developed to explore the dependence of gate characteristics in the linear regime on tube density and metallic contamination for thin films made of randomly oriented nanotubes. The on-off ratio before and after the breakdown of metallic tubes is analyzed and explained. The results presented here should be a powerful and unique predictive modeling capability for the analysis, design, and development not only of TFTs but in any two-component system with competing materials, e.g., metal CNT saturated organics[25] and organic photovoltaic applications.[26]

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